D PHYSICS

CSIR-NET, GATE, SET, JEST, IIT-JAM, BARC, TIFR

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Physical Science

ELECTRONICS

Previous Year Questions [Topic-Wise]

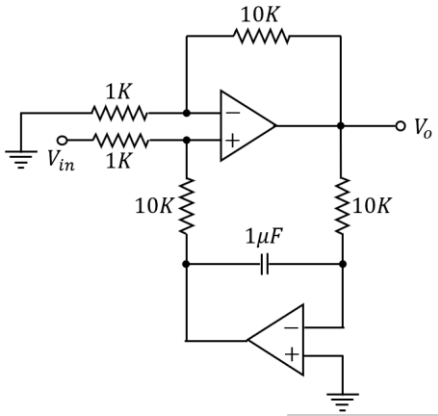
With Answer Key

CSIR-NET/JRF, GATE, JEST, TIFR

OP-AMP

❖ CSIR-NET PYQ

1. A time varying signal V_{in} is fed to an op-amp circuit with output signal V_0 as shown in the figure below.
The circuit implements a **[CSIR-JUNE 2011]**



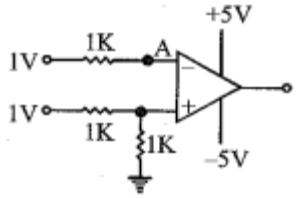
(a) High pass filter with cutoff frequency 16 Hz.

(b) High pass filter with cutoff frequency 100 Hz

(c) Low pass filter with cutoff frequency 16 Hz

(d) Low pass filter with cutoff frequency 100 Hz.

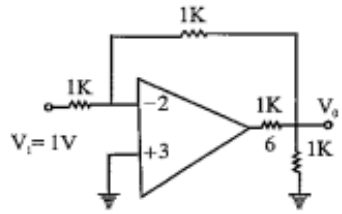
2. In the operational amplifier circuit below, the voltage at point A is
[CSIR-DEC 2011]



(a) 1.0 V (b) 0.5 V

(c) 0 V (d) −5.0 V

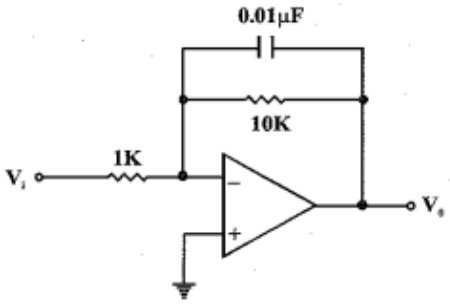
3. In the op-amp circuit shown in the figure below, the input voltage V_i is $1V$. The value of the output V_0 is **[CSIR-JUNE 2012]**



(a) −0.33 V (b) −0.50 V

(c) −1.00 V (d) −0.25 V

4. In the op-amp circuit shown in the figure, V_i is a sinusoidal input signal of frequency 10 Hz and V_0 is the output signal.



The magnitude of the gain and the phase shift, respectively, are close to the values
[CSIR-DEC 2012]

(a) $5\sqrt{2}$ and $\frac{\pi}{2}$ (b) $5\sqrt{2}$ and $\frac{-\pi}{2}$

(c) 10 and zero (d) 10 and π

5. Band-pass and band-reject filters can be implemented by combining a low pass and a high pass filter in series and in parallel, respectively. If the cut-off frequencies of the low pass and high pass filters are ω_0^{LP} and ω_0^{HP}, respectively, the condition required to implement the band-pass and band-reject filters are respectively.
[CSIR-DEC 2012]

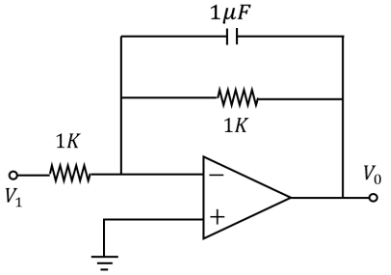
(a) $\omega_0^{HP} < \omega_0^{LP}$ and $\omega_0^{HP} < \omega_0^{LP}$

(b) $\omega_0^{HP} < \omega_0^{LP}$ and $\omega_0^{HP} > \omega_0^{LP}$

(c) $\omega_0^{HP} > \omega_0^{LP}$ and $\omega_0^{HP} < \omega_0^{LP}$

(d) $\omega_0^{HP} > \omega_0^{LP}$ and $\omega_0^{HP} > \omega_0^{LP}$

6. Consider the op-amp circuit shown in the figure.
If the input is a sinusoidal wave $V_i = 5\sin(1000t)$, then the amplitude of the output V_0 is **[CSIR-DEC 2013]**



(a) $\frac{5}{2}$ (b) 5

(c) $\frac{5\sqrt{2}}{2}$ (d) $5\sqrt{2}$

7. An op-amp based voltage follower

[CSIR-JUNE 2014]

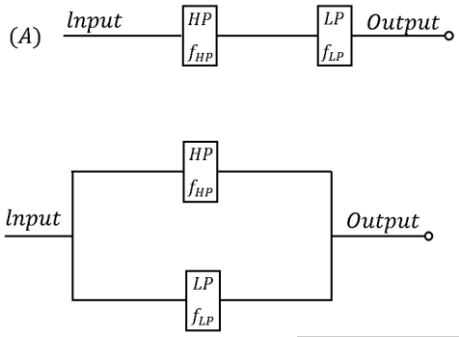
(a) is useful for converting a low impedance source into a high impedance source

(b) is useful for converting a high impedance source into a low impedance source

(c) has infinitely high closed loop output impedance

(d) has infinitely high closed loop gain

8. Consider a Low Pass (LP) and a High Pass (HP) filter with cut-off frequencies f_{LP} and f_{HP} respectively, connected in series or in parallel configurations as shown in the Figures A and B below.



Which of the following statements is correct?

[CSIR-DEC 2014]

(a) For $f_{HP} < f_{LP}$, A acts as a Band Pass filter and B acts as a Band Reject filter

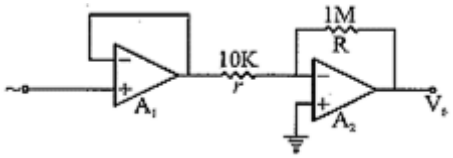
(b) For $f_{HP} > f_{Lp}$, A stops the signal from passing through and B passes the signal without filtering

(c) For $f_{HP} < f_{LP}$, A acts as a Band Pass filter and B passes the signal without filtering

(d) For $f_{HP} > f_{LP}$, A passes the signal without filtering and B acts as a Band Reject filter

9. Consider the amplifier circuit comprising of the two op-amps A_1 and A_2 as shown in the figure If the input ac signal source has an impedance of 50kΩ, which of the following statements is true?

[CSIR-DEC 2014]



(a) A_1 is required in the circuit because the source impedance is much greater than r

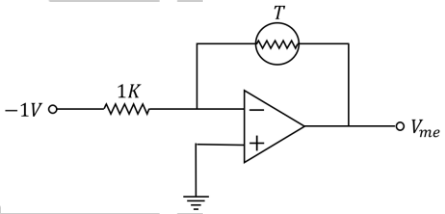
(b) A_1 is required in the circuit because the source impedance is much less than R

(c) A_1 can be eliminated from the circuit without affecting the overall gain

(d) A_I is required in the circuit if the output has to follow the phase of the input signal

10. In the circuit given below, the thermistor has a resistance 3kΩ at 25°C. Its resistance decreases by 150Ω per °C upon heating. The output voltage of the circuit at 30°C is

[CSIR-JUNE 2015]

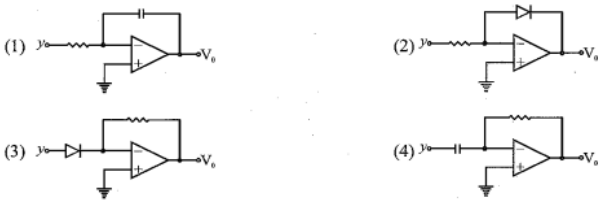


(a) −3.75 V (b) −2.25 V

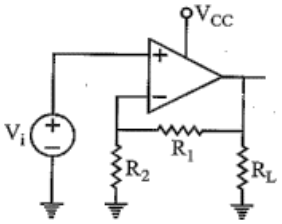
(c) 2.25 V (d) 3.75 V

11. If the parameters y and x are related by $y = \log(x)$, then the circuit that can be used to produce an output voltage V_0 varying linearly with x is

[CSIR-DEC 2015]



12. In the circuit below, the input voltage V_i is 2 V, $V_{cc} = 16$ V, $R_2 = 2$kΩ and $R_L = 10$kΩ.

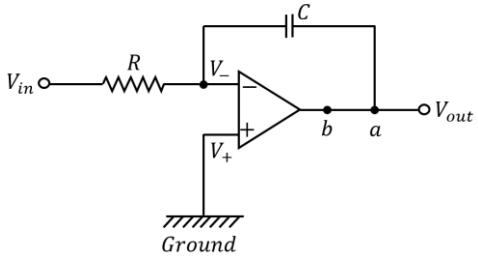


The value of R_f required to deliver 10 mW of power across R_L is **[CSIR-DEC 2016]**

(a) 12kΩ (b) 4Kω

(c) 8kΩ (d) 14kΩ

13. The gain of the circuit given below is $-\frac{1}{\omega RC}$.



The modification in the circuit required to introduce a dc feedback is to add a resistor **[CSIR-JUNE 2017]**

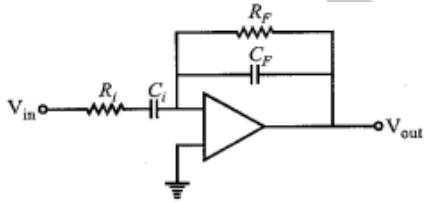
(a) between a and b

(b) between positive terminal of the op-amp and ground

(c) in series with C

(d) parallel to C

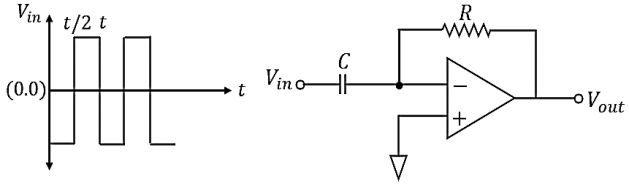
14. In the following operational amplifier circuit $C_{\text{in}} = 10\text{nF}, R_{\text{tn}} = 20\text{k}\Omega, R_F = 200\text{k}\Omega$ and $C_F = 100\text{pF}$.
The magnitude of the gain at a input signal frequency of 16kHz is **[CSIR-JUNE 2017]**

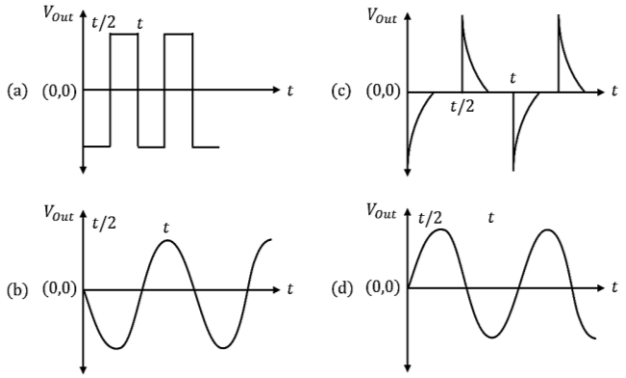


(a) 67 (b) 0.15

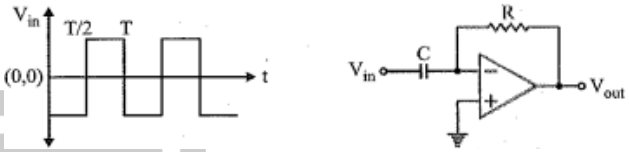
(c) 0.3 (d) 3.5

15. The input V_i to the following circuit is a square wave as shown in the following figure:
Which of the waveforms V_o best describes the output? **[CSIR-JUNE 2018]**

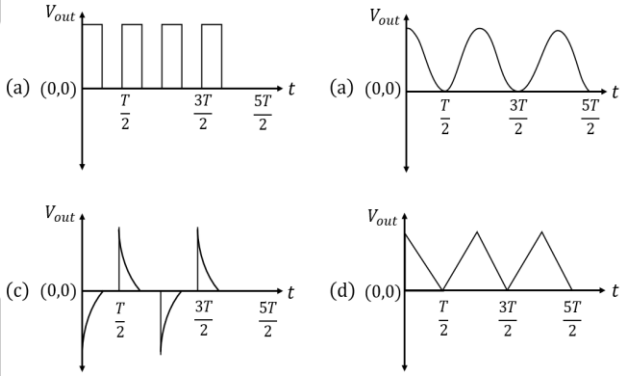




16. The input V_i to the following circuit is a square wave as shown in the following figure.
[CSIR-DEC 2018]



Which of the waveforms best describes the output?



17. For optimal performance of an op-amp based current-to-voltage converter circuit, the input and output impedance should be **[CSIR-JUNE 2019]**

(a) low input impedance and high output impedance

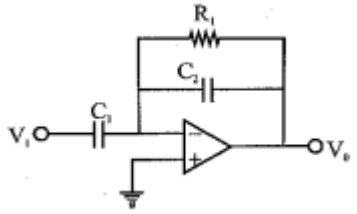
(b) low input impedance and low output impedance

(c) high input impedance and high output impedance

(d) high input impedance and low output impedance

18. A circuit constructed using op-amp, resistor $R_1 = 1\text{k}\Omega$ and capacitors $C_1 = 1\mu F$ and $C_2 =$

$0.1\mu F$, is shown in the figure below.

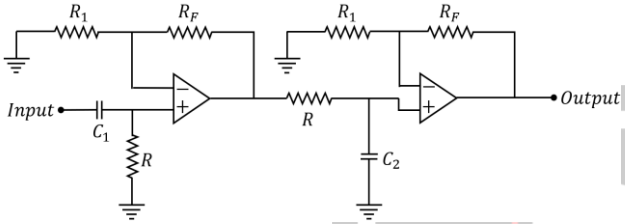


This circuit will act as a **[CSIR-JUNE 2019]**

(a) high pass filter (b) low pass filter

(c) band pass filter (d) band reject filter

19. In the circuit diagram of a band pass filter shown below, $R = 10\text{k}\Omega$.



In order to get a lower cut-off frequency of 150 Hz and an upper cut-off frequency of 10kHz, the appropriate values of C_1 and C_2 respectively are **[CSIR-DEC 2019]**

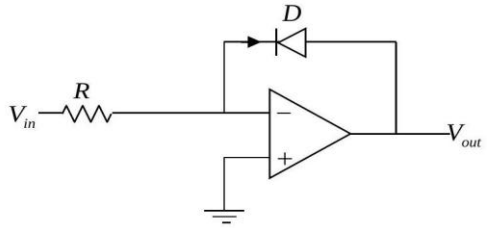
(a) 0.1μF and 1.5nF (b) 0.3μF and 5.0nF

(c) 1.5nF and 0.1μF (d) 5.0nF and 0.3μF

20. The $I-V$ characteristics of the diode D in the circuit below is given by

$$I = I_s\left(e^{\frac{qV}{k_BT}} - 1\right)$$

where I_s is the reverse saturation current, V is



the voltage across the diode and T is the absolute temperature. If the input voltage is V_{in}, then the output voltage V_{out} is **[CSIR-JUNE 2020]**

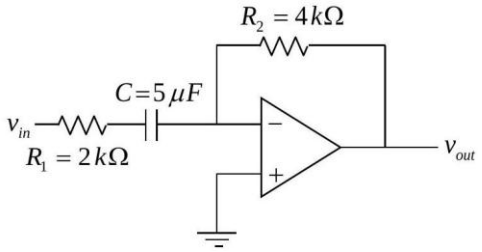
(a) $I_S R \ln\left(\frac{qV_{\text{in}}}{k_BT} + 1\right)$

(b) $\frac{1}{q}k_BT \ln\left(\frac{q(V_{in} + I_SR)}{k_BT}\right)$

(c) $\frac{1}{q}k_BT \ln\left(\frac{V_{\text{in}}}{I_SR} + 1\right)$

(d) $-\frac{1}{q}k_BT\ln\left(\frac{V_{in}}{I_SR} + 1\right)$

21. In the circuit shown below, the gain of the op-amp in the middle of its bandwidth is 10^5. A sinusoidal voltage with angular frequency $\omega = 100\text{rad/s}$ is applied to the input of the op--amp.

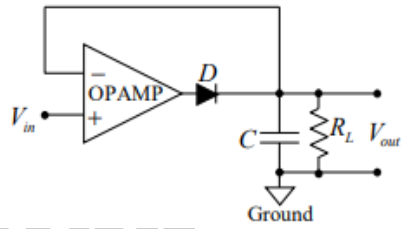


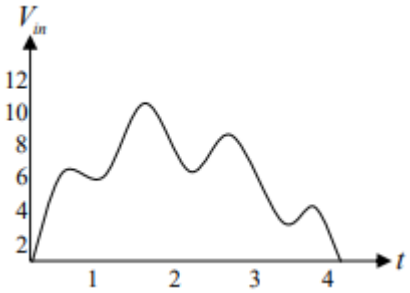
The phase difference between the input and the output voltage is **[CSIR-JUNE 2020]**

(a) $5\pi/4$ (b) $3\pi/4$

(c) $\pi/2$ (d) π

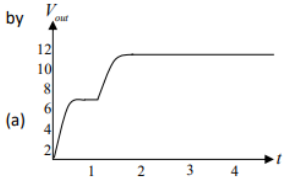
22. In the following circuit the input voltage V_{in} is such that $|V_{\text{in}}| < |V_{\text{out}}|$, where V_{sat} is the saturation voltage of the op-amp. (Assume that the diode is an ideal one and R_LC is much large than the duration of the measure

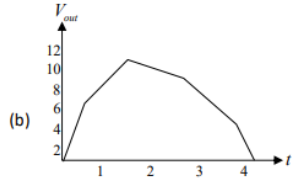




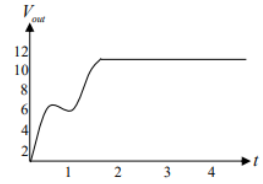
for the input voltage as shown in the figure above, the output voltage V_{out} is best represented by **[CSIR-JUNE 2021]**

by

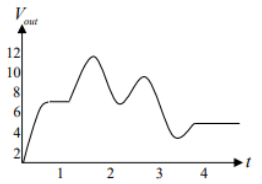




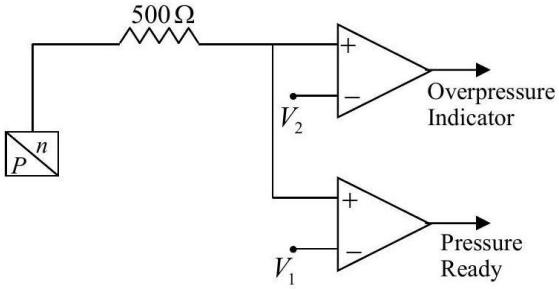
(c)



(d)



23. The pressure of a gas in a vessel needs be maintained between 1.5 bar to 2.5 bar in an experiment. The vessel is fitted with a pressure transducer that generates 4 mA to 20 mA current for pressure in the range 1 bar to 5 bar. The current output of the transducer has a linear dependence on the pressure.

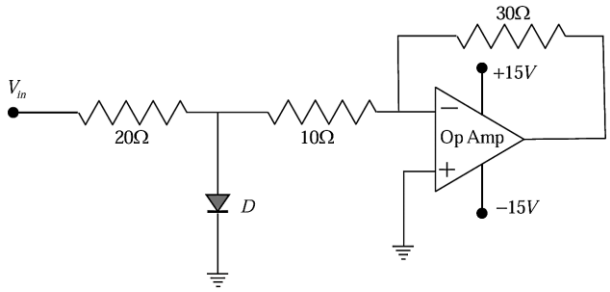


The reference voltages V_1 and V_2 in the comparators in the circuit (shown in figure above) suitable for the desired operating conditions, are, respectively **[CSIR-JUNE 2021]**

(a) 2 V and 10 V (b) 2 V and 5 V

(c) 3 V and 10 V (d) 3 V and 5 V

24. In the circuit below, there is a voltage drop of 0.7 V across the diode in forward bias while no current flows through it in reverse bias.

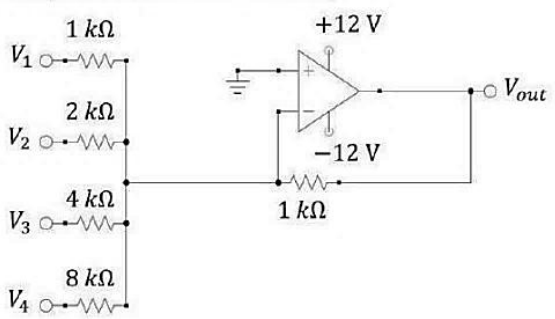


In V_{in} is a sinusoidal signal of frequency 50 Hz with rms value of 1 V the maximum current that flows through the diode is closest to

(a) 1A (b) 0.14 A

(c) 0 A (d) 0.07 A

25. In the circuit shown below using an ideal op amp, inputs $V_j (j = 1,2,3,4)$ may either be open or connected to a -5 V battery.

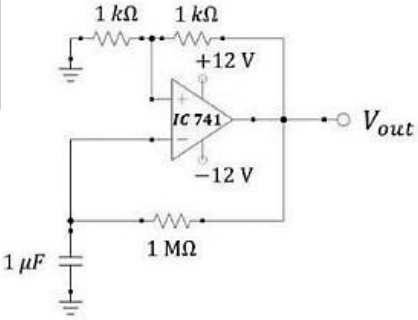


The minimum measurement range of a voltmeter to measure all possible values of V_{out} is **[CSIR-DEC 2023]**

(a)10 V (b)30 V

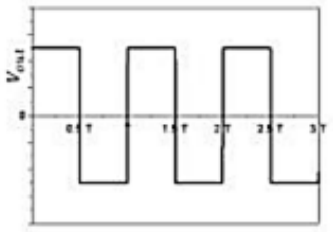
(c)3 V (d)1 V

26. A circuit with operational amplifier is shown in the figure below.

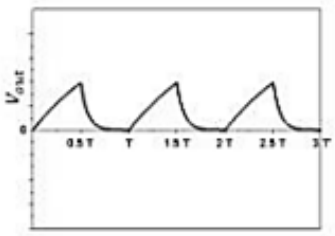


The output voltage waveform V_{out} will be closest to **[CSIR-DEC 2023]**

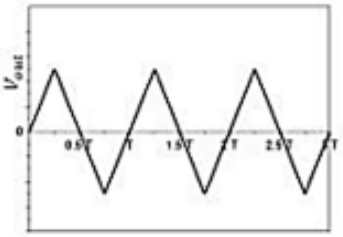
1.



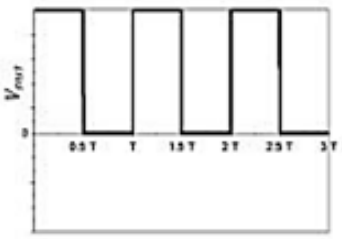
2.



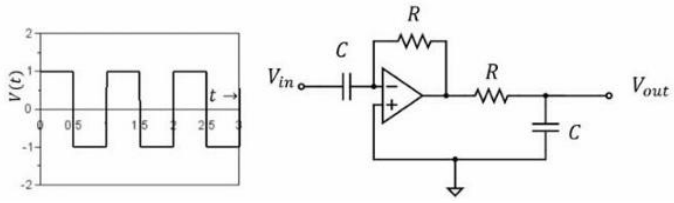
3.



4.



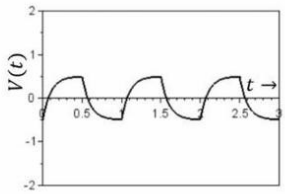
27. A train of square wave pulses is given to the input of an ideal opamp circuit shown below.



Given that the time period of the input pulses $T \ll RC$ and the opamp does not get into saturation, which of the following best represents the output waveform?

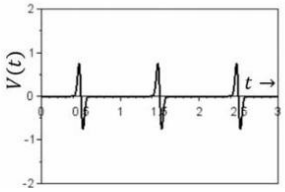
[CSIR-JUNE 2024]

1.

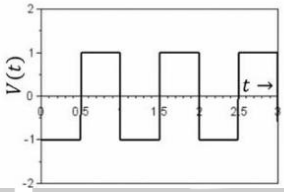


2.

3.

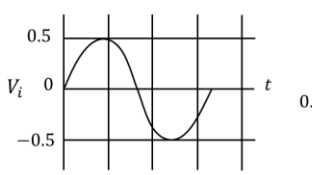


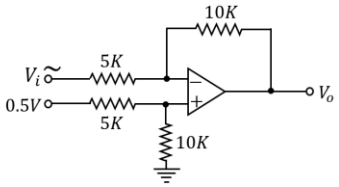
4.



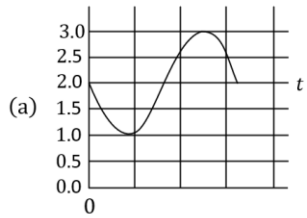
28. Given the input voltage V_i, which of the following waveforms correctly represents the output voltage V_0 in the circuit shown below ?

[CSIR-JUNE 2016]

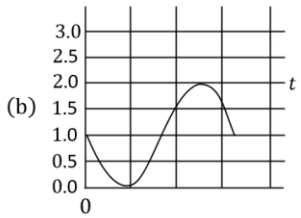




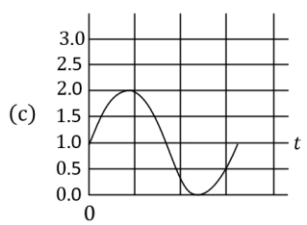
(a)



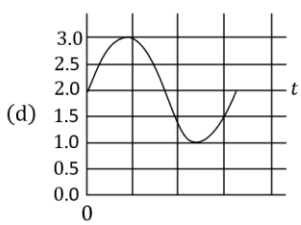
(b)



(c)



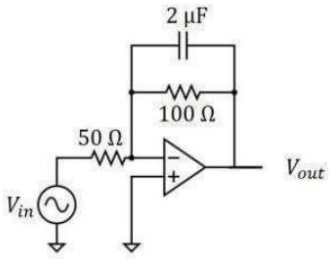
(d)



29. In the circuit shown below, the input voltage (in volts) is given by

$$V_{in}(t) = 0.1\sin(\omega_1 t) + \sin(\omega_2 t)$$

where $\omega_1 = 5 \times 10^2\ \text{s}^{-1}$ and $\omega_2 = 5 \times 10^4\ \text{s}^{-1}$.



The time varying part of the output voltage $V_{\text{out}}(t)$ (in volts) is closest to **[CSIR DEC 2024]**

(a) $-0.2\sin(\omega_1 t) - 2\sin(\omega_2 t)$

(b) $-0.2\sin(\omega_1 t) + 0.2\cos(\omega_2 t)$

(c) $2\cos(\omega_1 t) + 0.2\cos(\omega_2 t)$

(d) $2\cos(\omega_1 t) - 2\sin(\omega_2 t)$

❖ GATE PYQ

1. The inverting input terminal of an operational amplifier (op-amp) is shorted with the output terminal apart from being grounded. A voltage signal v_i is applied to the non-inverting input terminal of the op-amp. Under this configuration, the op-amp functions as **[GATE 2004]**

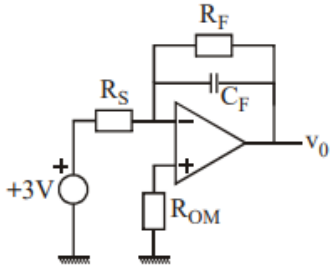
(a) an open loop inverter

(b) a voltage to current converter

(c) a voltage follower

(d) an oscillator

2. Figure shows a practical integrator with $R_S = 30\text{M}\Omega$, $R_F = 20\text{M}\Omega$ and $C_F = 0.1\mu\text{F}$. If a step (dc) voltage of $+3$ V is applied as input for $0 \le t \le 4$ (t is in seconds), the output voltage is **[GATE 2004]**



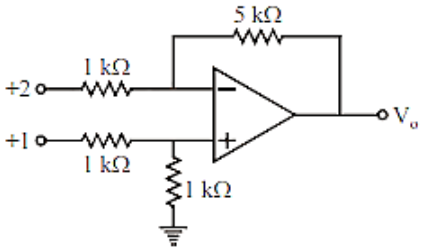
(a) a ramp function of -6 V

(b) a step function of -12 V

(c) a ramp function of -15 V

(d) a ramp function of -4 V

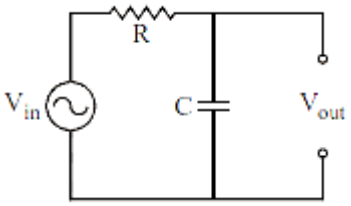
3. The output V_0 of the ideal opamp circuit shown in the figure is **[GATE 2005]**



(a) -7 V (b) -5 V

(c) 5 V (d) 7 V

4. The circuit shown in the figure can be used as a **[GATE 2005]**



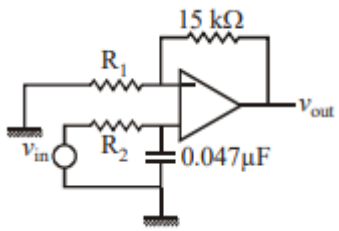
(a) high pass filter or a differentiator

(b) high pass filter or an integrator

(c) low pass filter or a differentiator

(d) low pass filter or an integrator

5. The low-pass active filter shown in the figure has a cut-off frequency of 2kHz and a pass band gainof 1.5. The values of the resistors are **[GATE 2006]**



(a) $R_1 = 10\text{k}\Omega; R_2 = 1.3\Omega$

(b) $R_1 = 30\text{k}\Omega; R_2 = 1.3\Omega$

(c) $R_1 = 10\text{k}\Omega; R_2 = 1.7\Omega$

(d) $R_1 = 30\text{k}\Omega; R_2 = 1.7\Omega$

6. In order to obtain a solution of the differential equation $\frac{d^2v}{dt^2} - 2\frac{dv}{dt} + v_1 = 0$, involving voltages $v(t)$ and v_1, an operational amplifier (Op-Amp) circuit would require at least **[GATE 2006]**

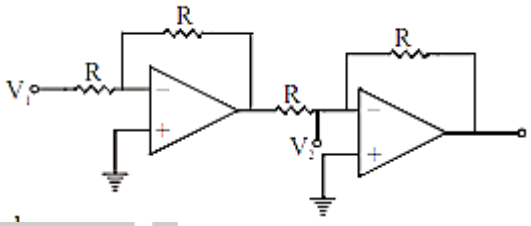
(a) two Op-Amp integrators and one Op-Amp adder

(b) two Op-Amp differentiators and one Op-Amp adder

(c) one Op-Amp integrator and one Op-Amp adder

(d) one Op-Amp integrator, one Op-Amp differentiator and one Op-Amp adder

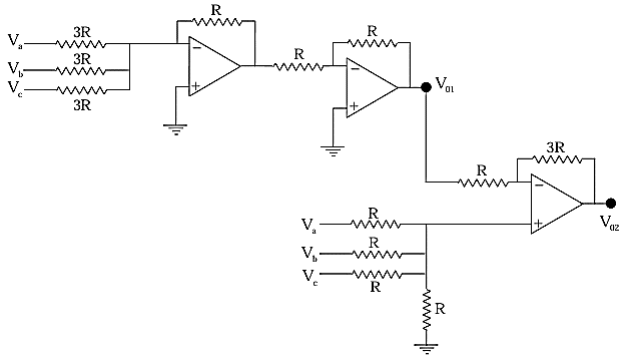
7. The circuit shown is based on ideal operational amplifiers. It acts as a **[GATE 2007]**



(a) subtractor (b) buffer amplifier

(c) adder (d) divider

Statement for Linked Answer Questions 8 &9:
The following circuit contains three operational amplifiers and resistors.



8. The output voltage at the end of second operational amplifier V_{01} is **[GATE 2008]**
(a) $V_{01} = 3(V_a + V_b + V_c)$

(b) $V_{01} = -\frac{1}{3}(V_a + V_b + V_c)$

(c) $V_{01} = \frac{1}{3}(V_a + V_b + V_c)$

(d) $V_{01} = \frac{4}{3}(V_a + V_b + V_c)$

9. The output V_{02} (at the end of third op amp) of the above circuit is **[GATE 2008]**

(a) $V_{02} = 2(V_a + V_b + V_c)$

(b) $V_{02} = 3(V_a + V_b + V_c)$

(c) $V_{02} = -\frac{1}{2}(V_a + V_b + V_c)$

(d) zero

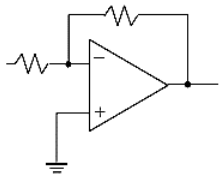
10. The Common Mode Rejection Ratio (CMRR) of a differential amplifier using an operational amplifier is 100 dB. The output voltage for a differential input of 200μV is 2 V. The common mode gain is **[GATE 2009]**

(a) 10 (b) 0.1

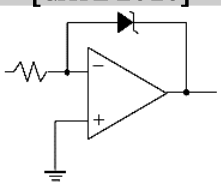
(c) 30 Db (d) 10 dB

11. In one of the following circuits, negative feedback does not operate for a negative input. Which one is it? The op-amps are running from $\pm$15 V supplies. **[GATE 2010]**

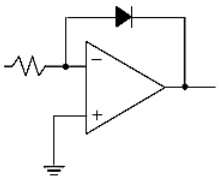
(A)



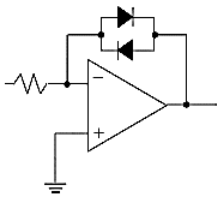
(B)



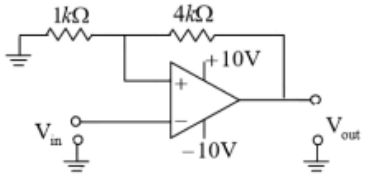
(C)



(D)

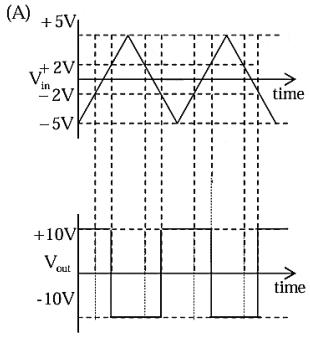


12. Consider the following circuit

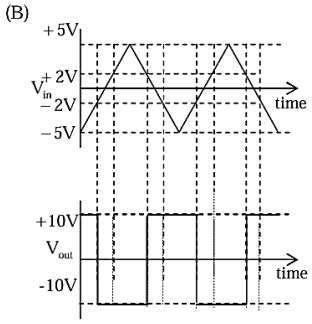


Which of the following correctly represent the output V_{out} corresponding to the input V_{in} ? **[GATE 2011]**

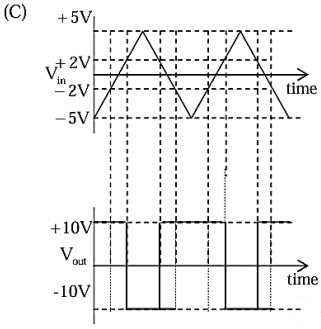
(A)



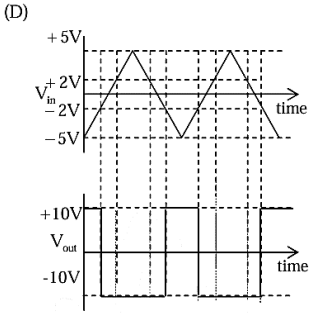
(B)



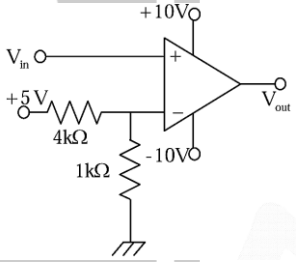
(C)



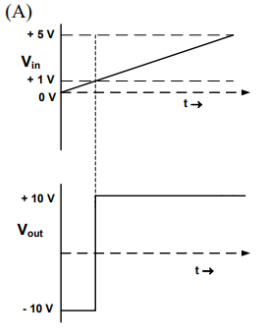
(D)



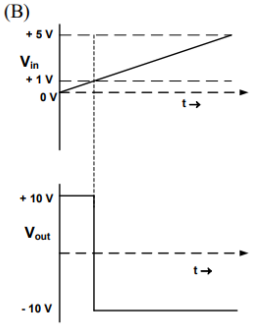
13. Consider the following OP-AMP circuit **[GATE 2012]**



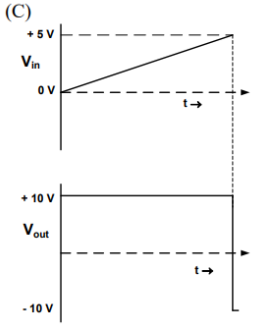
(A)



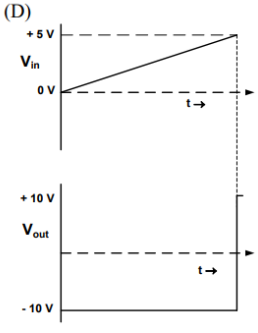
(B)



(C)

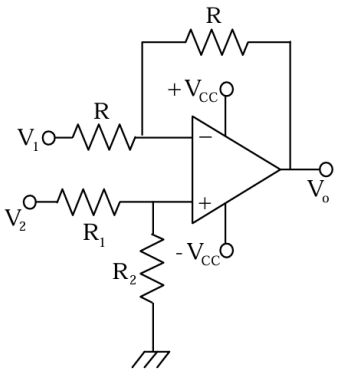


(D)



14. In the following circuit, for the output voltage to be $V_0 = (-V_1 + V_2/2)$, the ratio R_1/R_2 is

[GATE 2012]

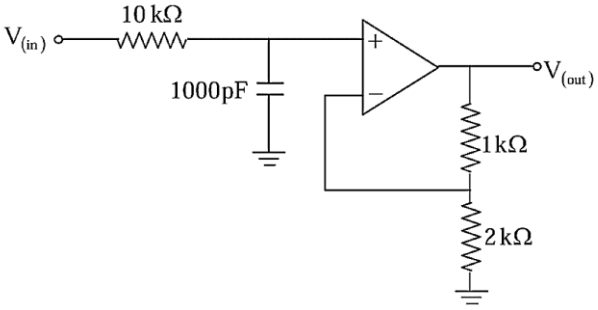


(a) ½ (b) 1

(c) 2 (d) 3

Statement for Linked Answer Questions 15 and 16: Consider the following circuit

[GATE 2013]



15. For this circuit the frequency above which the gain will decreases by 20 dB per decade is

(a) 15.9kHz (b) 1.2kHz

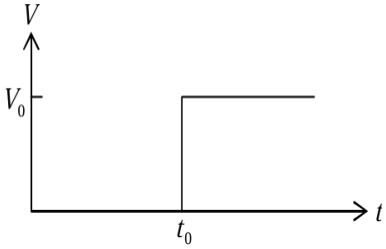
(c) 5.6kHz (d) 22.5kHz

16. At 1.2kHz the closed loop gain is

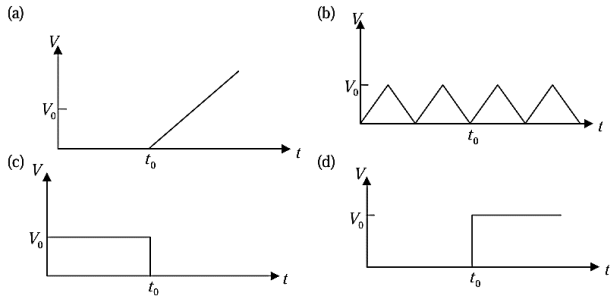
(a) 1 (b) 1.5

(c) 3 (d) 0.5

17. The input given to an ideal OP-AMP integrator circuit is **[GATE 2014]**



The correct output of the integrator circuit is



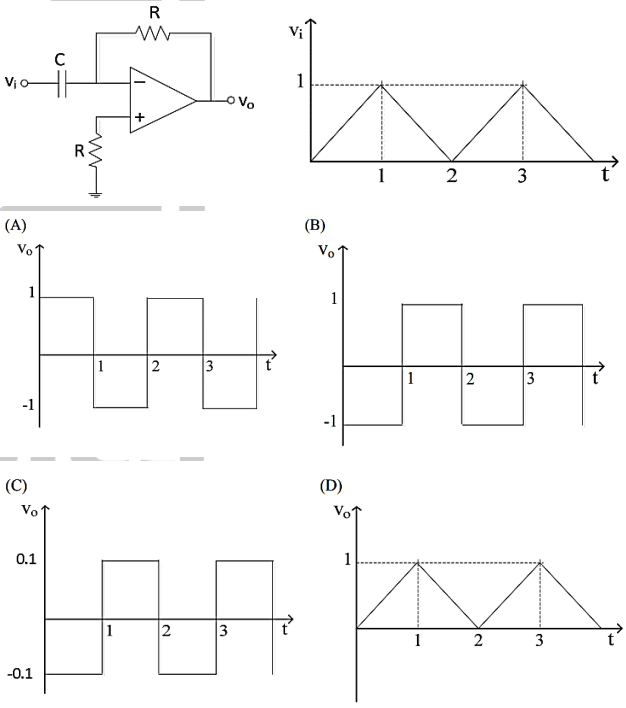
18. A low pass filter is formed by a resistance R and a capacitance C. At the cut off angular frequency $\omega_c = \frac{1}{RC}$, the voltage gain and the phase of the output voltage relative to the input voltage respectively are **[GATE 2014]**

(a) 0.71 and 45° (b) 0.71 and −45°

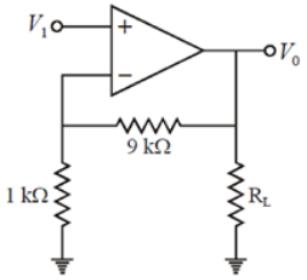
(c) 0.5 and −90° (d) 0.5 and 90°s

19. Consider the circuit shown in the figure, where RC = 1. For an input signal V_i shown below, choose the correct V_0 from the options:

[GATE 2015]



20. In the given circuit, if the open loop gain $A = 10^5$, the feedback configuration and the closed loop gain A_f are **[GATE 2015]**



(a) series-shunt, $A_f = 9$

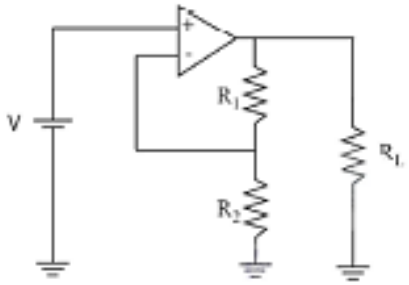
(b) series-series, $A_f = 10$

(c) series-shunt, $A_f = 10$

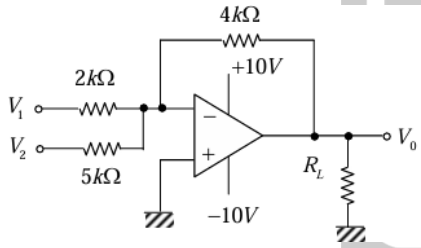
(d) shunt-shunt, $A_f = 10$

21. Consider an ideal operational amplifier as shown in the figure below with $R_1 = 5k\Omega, R_2 = 1k\Omega, R_L = 100k\Omega$. For an applied input voltage $V = 10$mV, the current passing through R_2 is_____ μA. (up to two decimal places)

[GATE 2017]

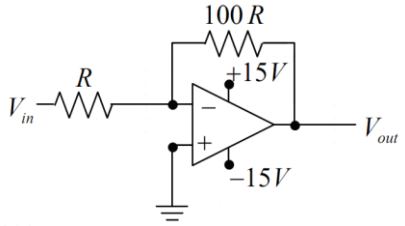


22. For an operational amplifier (ideal) circuit shown below,



If $V_1 = 1V$ and $V_2 = 2V$, the value of V_0 is V (up to one decimal place). **[GATE 2018]**

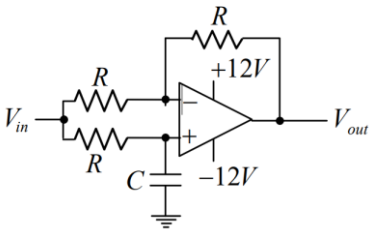
23. For the following circuit, what is the magnitude of V_{out} if $V_{in} = 1.5$ V ? **[GATE 2019]**



(a) 0.015 V (b) 0.15 V

(c) 15 V (d) 150 V

24. The input voltage (V_{in}) to the circuit shown in the figure is $2\cos(100t)V$. The output voltage (V_{out}) is $2\cos\left(100t - \frac{\pi}{2}\right)V$. If $R = 1k\Omega$, the value of C (in μF)is **[GATE 2020]**



(a) 0.1 (b) 1

(c) 10 (d) 100

25. For an Op-Amp based negative feedback, non-inverting amplifier, which of the following statements are true?

[GATE 2022]

(a) Closed loop gain < Open loop gain

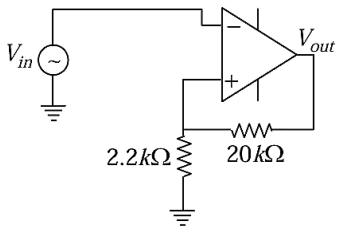
(b) Closed loop bandwidth < Open loop bandwidth

(c) Closed loop input impedance > Open loop input impedance

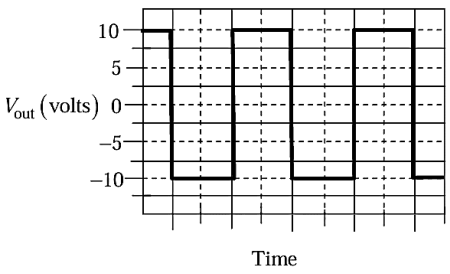
(d) Closed loop output impedance < Open loop output impedance

26. For the Op-Amp circuit shown below, choose the correct output waveform corresponding to the input $V_{in} = 1.5\sin 20\pi t$ (in Volts). The saturation voltage for this circuit is $V_{\text{sat}} = \pm 10$ V.

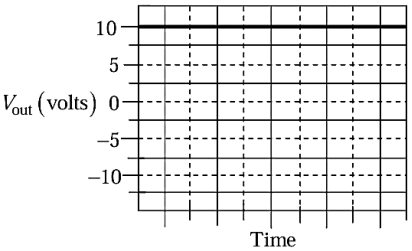
[GATE 2022]



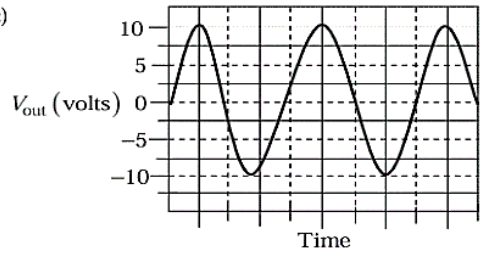
(a)



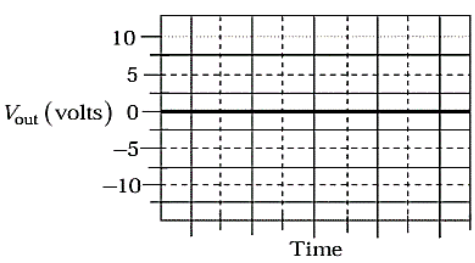
(b)



(c)

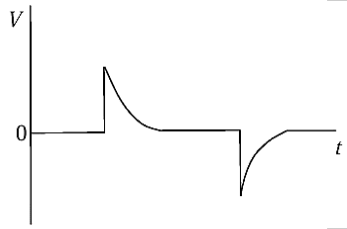


(d)

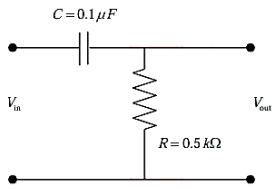


27. An input voltage in the form of a square wave of frequency 1kHz is given to a circuit, which results in the output shown schematically below. Which one of the following options is the CORRECT representation of the circuit?

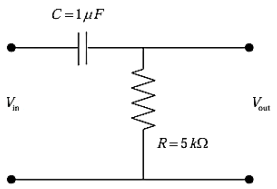
[GATE 2023]



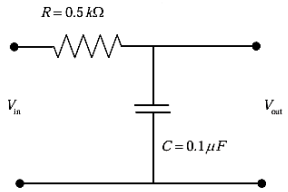
(A)



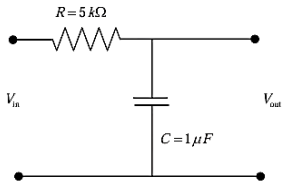
(B)



(C)

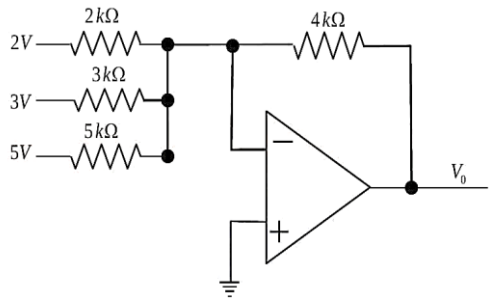


(D)



28. Consider the operational amplifier circuit shown in figure.

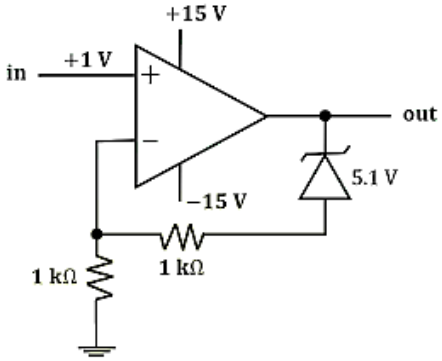
[GATE 2024]



The output voltage V_0 is V (integer).

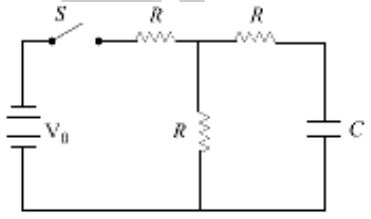
29. The figure shows an opamp circuit with a 5.1 V Zener diode in the feedback loop. The opamp runs from ± 15 V supplies. If a $+1$ V signal is applied at the input, the output voltage (rounded off to one decimal place) is

[GATE 2025]



❖ JEST PYQ

1. A capacitor C is connected to a battery V_0 through three equal resistors R and a switch S as shown below:



The capacitor is initially uncharged. At time $t = 0$, the switch S is closed. The voltage across the capacitor as a function of time ' t ' for $t > 0$ is given by **[JEST 2012]**

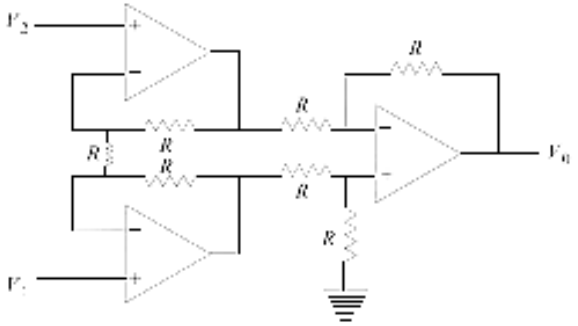
(a) $(V_0/2)(1 - \exp(-t/2Rc))$

(b) $(V_0/3)(1 - \exp(-t/3Rc))$

(c) $(V_0/3)(1 - \exp(-3t/2Rc))$

(d) $(V_0/2)(1 - \exp(-2t/3Rc))$

2. The classic three op-amp instrumentation amplifier configuration is shown below:



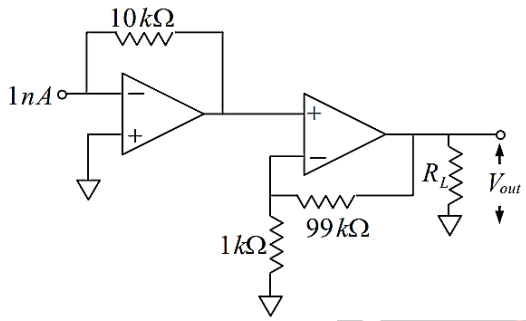
The op-amp are ideal and all resistors are of equal value R. The gain, defined as the output voltage V_0 divided by the differential input voltage $V_1 - V_2$, is equal to **[JEST 2012]**

(a) 2 (b) 3

(c) 4 (d) 6

3. What is the voltage at the output of the following operational amplifier circuit [see figure 1]?

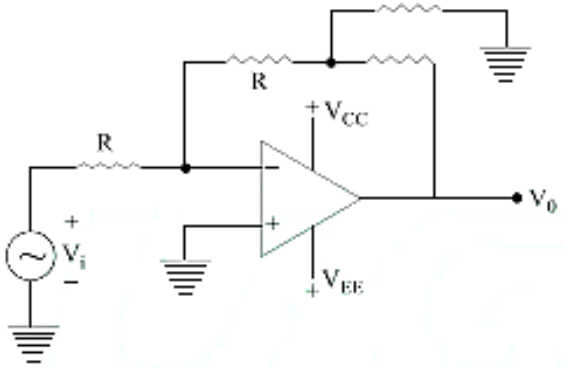
[JEST 2015]



(a) 1 V (b) 1Mv

(c) 1μV (d) 1Nv

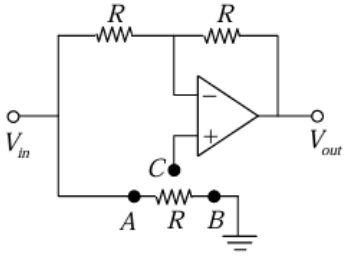
4. Consider a 741 operational amplifier circuit as shown below, where $V_{CC} = V_{EE} = +15V$ and $R = 2.2k\Omega$. If $V_1 = 2$mV, what is the value of V_0 with respect to the ground? **[JEST 2017]**



(a) -1mV (b) -2mV

(c) -3mV (d) -4mV

5. Analysis the ideal op-amp circuit in the figure. Which one of the following statements is true about the output voltage V_{out}, when terminal 'C' is connected to point 'A' and then to point 'B'? **[JEST 2019]**



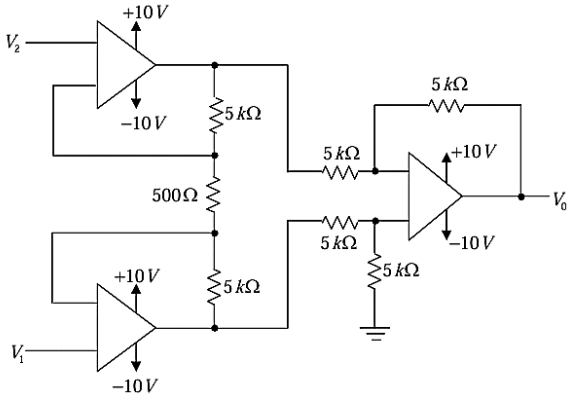
(a)$V_{\text{out}} = V_{\text{in}}$ and $V_{\text{out}} = -V_{\text{in}}$ when 'C' is connected to 'A' and 'B', respectively

(b) $V_{\text{out}} = -V_{\text{in}}$ and $V_{\text{out}} = V_{\text{in}}$ when 'C' is connected to 'A' and 'B', respectively

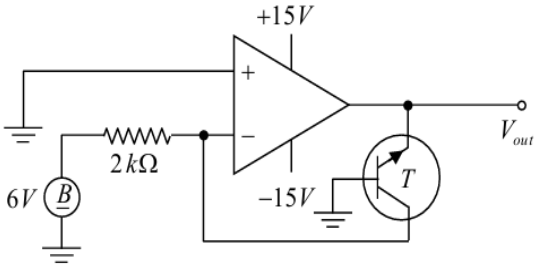
(c) $V_{\text{out}} = -V_{\text{in}}$ when 'C' is connected to either 'A' or 'B'

(d) $V_{\text{out}} = V_{\text{in}}$ when 'C' is connected to either 'A' or 'B'

6. Analyse the op-amp circuit shown in the figure below. What is the output voltage (V_0) in millivolts if $V_1 = 2.5$ and $V_2 = 2.25$ V?



7. An ideal op-amp and a silicon transistor T are used in the following circuit. Find the output voltage V_{out} **[JEST 2021]**

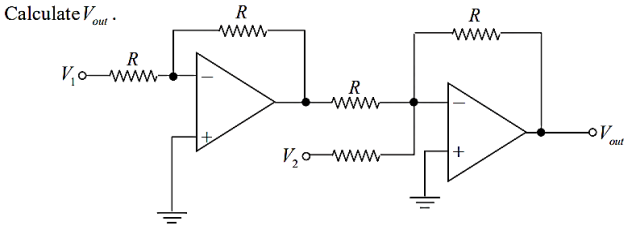


(a) +5.3 V (b) -0.7 V

(c) +0.7 V (d) -15 V

8. In the figure below with ideal op-amps, the value of $R = 10\text{k}\Omega$, $V_1 = -10$mV, and $V_2 = -30$mV.

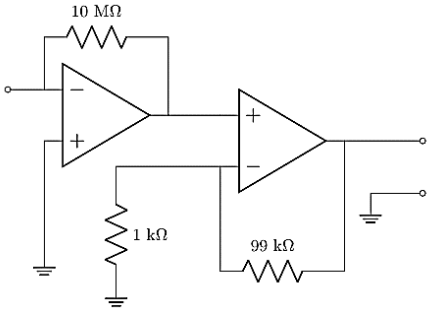
Calculate V_{out}. **[JEST 2021]**



(a) $+40mV$ (b) $-40mV$

(c) $+20mV$ (d) $-20mV$

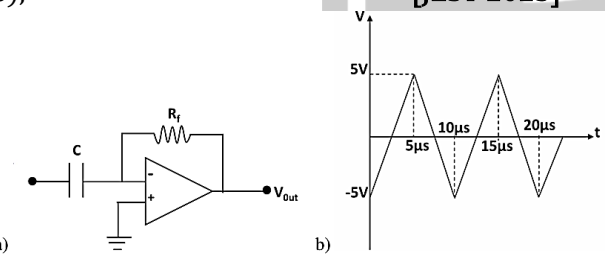
9. What is the output voltage of the following circuit for the input current 1nA ? **[JEST 2022]**



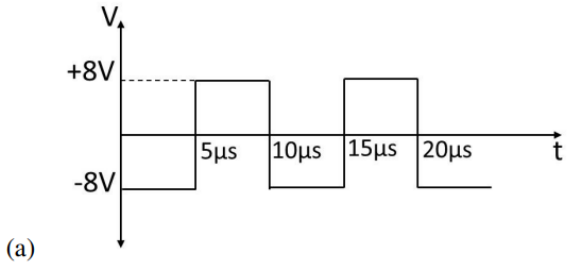
(a) 1mV (b) 1 V

(c) 1μV (d) 1Nv

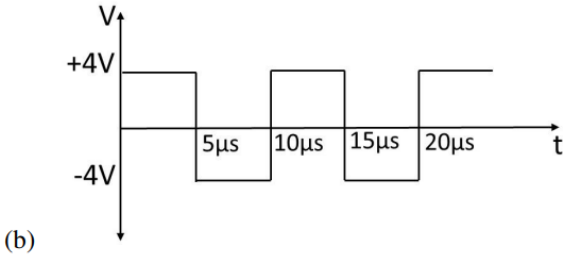
10. Consider the Op-Amp differentiator presented in Figure (a). Take $C = 0.002\mu$F and $R_f = 2$ kΩ. For a triangular wave input shown in the figure (b), **[JEST 2023]**



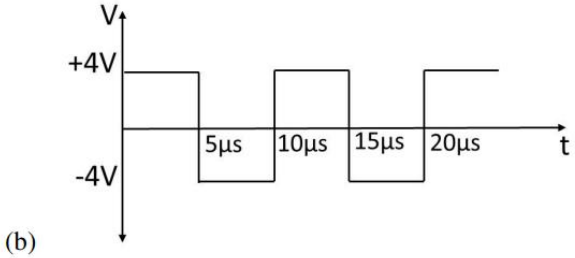
determine the output voltage waveform.



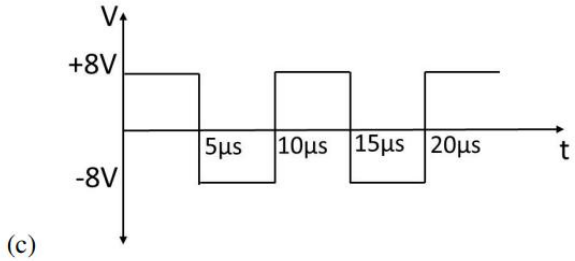
(a)



(b)

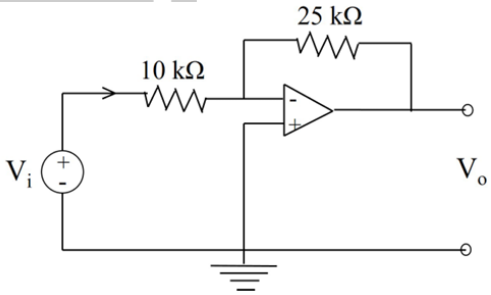


(b)



(c)

11. What is the output voltage V_o and current I in the 10kΩ resistance of the following circuit? $V_i = 0.5$ V. **[JEST 2024]**



(a) $V_o = -1.25$ V, $I = 20\mu$A

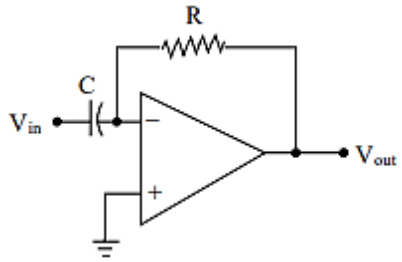
(b) $V_o = -0.4$ V, $I = 50\mu$A

(c) $V_o = -0.4$ V, $I = 20\mu$A

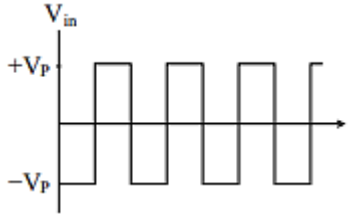
(d) $V_o = -1.25$V, $I = 50\mu$A

❖ **TIFR PYQ**

1. Consider the following circuit:

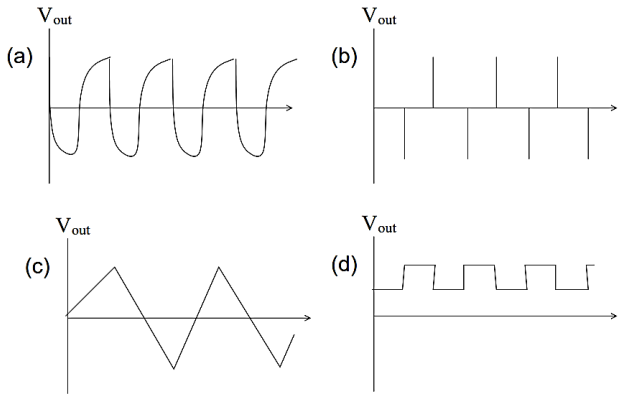


If the waveform given below is fed in at V_{in},

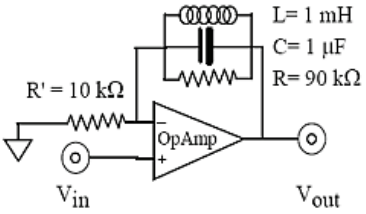


then the waveform at the output V_{out} will be

[TIFR 2012]



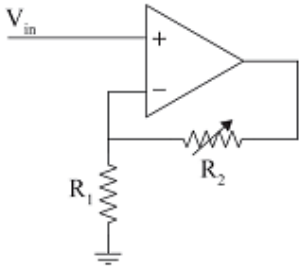
2. An input of 1.0 VDC is given to the ideal Op-Amp circuit depicted below. What will be the output voltage? **[TIFR 2013]**



(a) 10.0 V (b) −9.0 V

(c) 1.0 V v (d) 0 V

3. In the following circuit, the resistance R_2 is doubled.

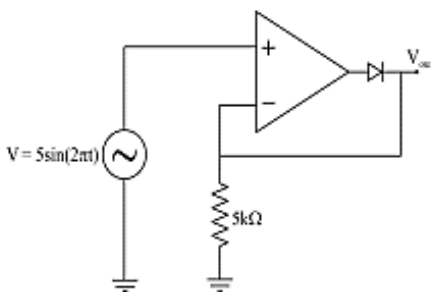


It follows that the current through R_2 **[TIFR 2014]**

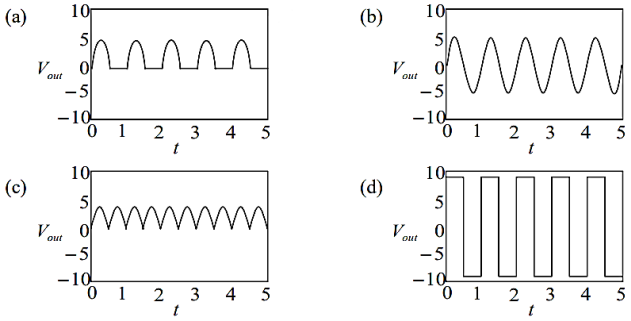
(a) remains the same. (b) is halved.

(c) is doubled. (d) is quadrupled.

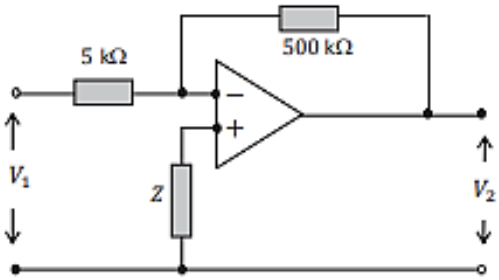
4. In the circuit shown below, the op-amp is powered by a bipolar supply of ± 10 V.



Which one of the following graphs represents V_{out} correctly? **[TIFR 2015]**



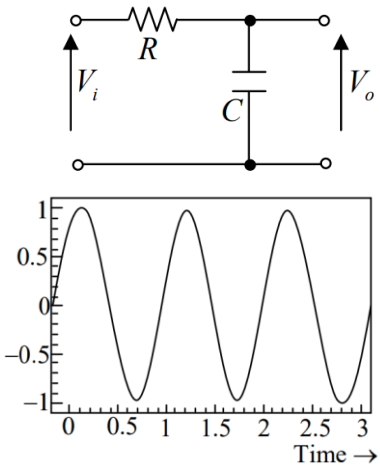
5. In the generalized operational amplifier circuit shown on the right, the op. amp. has a very high input impedance ($Z > 50\text{M}\Omega$) and an open gain of 1000 for the frequency range under consideration. Assuming that the op. amp. draws negligible current, the voltage ratio V_2/V_1 is approximately **[TIFR 2016]**



(a) -190 (b) -190

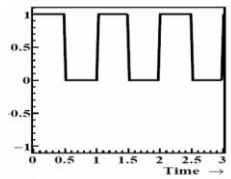
(c) -90 (d) 80

6. For the circuit depicted on the right, the input voltage V_i is a simple sinusoid as shown below, where the time period is much smaller compared to the time constant of this circuit. **[TIFR 2016]**

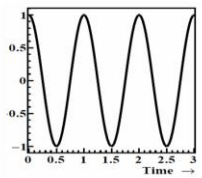


The voltage V_o across C is best represented by

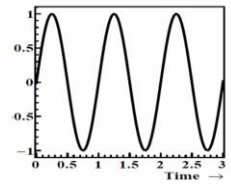
(a)



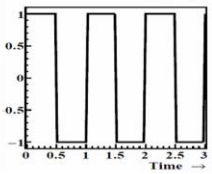
(b)



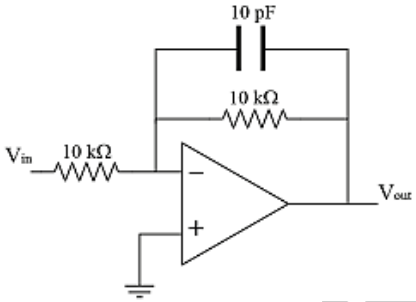
(c)



(d)



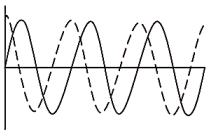
7. The following circuit is fed with an input sine wave of frequency 50 Hz.



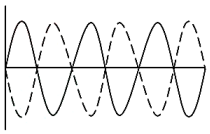
Which of the following graphs (solid line is input and dashed line is output) best represents the correct situation?

[TIFR 2017]

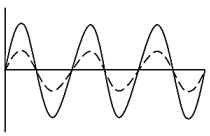
(a)



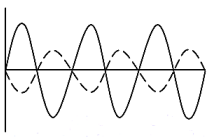
(b)



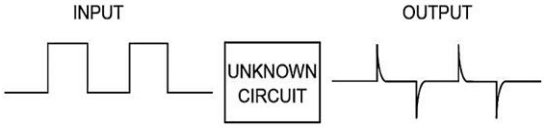
(c)



(d)



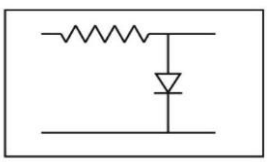
8. The figure below shows an unknown circuit, with an input and output voltage signal.



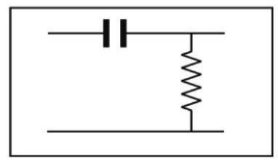
From the form of the input and output signals, one can infer that the circuit is likely to be

[TIFR 2018]

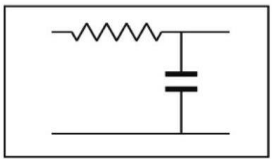
(a)



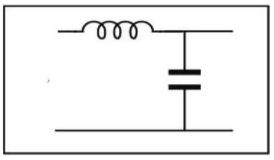
(b)



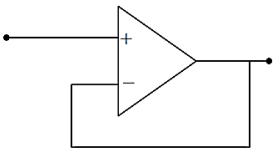
(c)



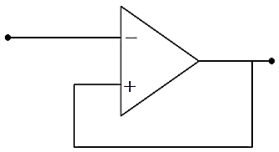
(d)



9. Consider the following circuits C-1 and C-2.



C-1



C-2

You can apply the golden rules of an ideal op-amp to **[TIFR 2018]**

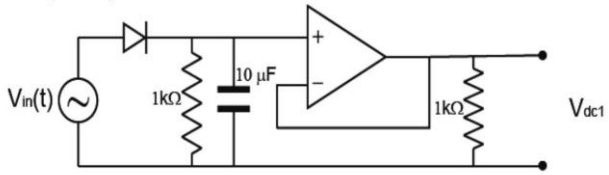
(a) only C − 1

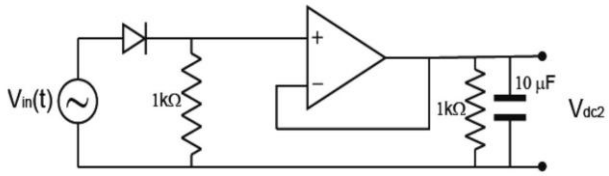
(b) only C-2

(c) both C-1 and C-2

(d) neither C-1 nor C-2

10. A signal $V_{in}(t) = 5\sin(100\pi t)$ is sent to both the circuits sketched below.





If the DC output voltage of the top circuit has a value V_{dc1} and the bottom circuit has a value V_{dc2}, then which of the following statements about the relative value of V_{dc1} and V_{dc2} is correct? **[TIFR 2018]**

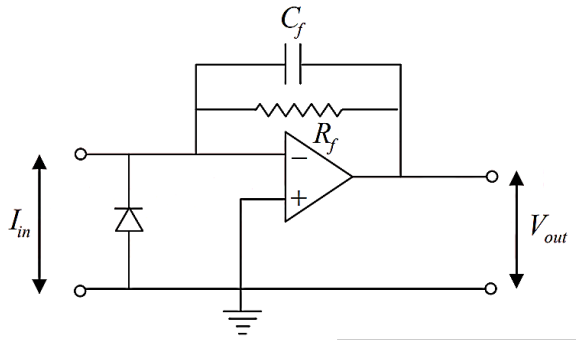
(a) $V_{dc1} < V_{dc2}$

(b)$V_{dc1} > V_{dc2}$

(c)$V_{dc1} = V_{dc2}$

(d) It will depend on the slew rate of the op-amp.

11. Consider the following circuit. **[TIFR 2019]**

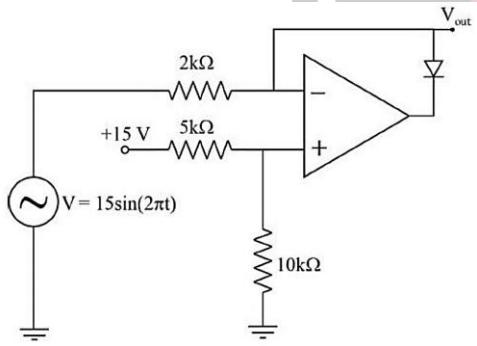


It is given that $C_f = 100$pF, and for $I_{\text{in}} = 50$nA D.C., $V_{\text{out}} = 1$ V D.C. Therefore, the bandwidth of the above circuit is

(a) 15.8 Hz (b) 79.6 Hz

(c) 145.3 Hz (d) 200.4 Hz

12. In the above circuit, which of the following is the maximum value, in Volts, of voltage at V_{out} ?

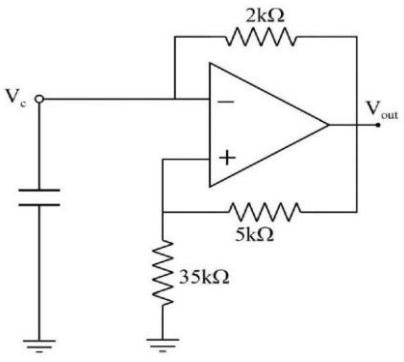


[TIFR 2020]

(a) 10 (b) 15

(c) 0 (d) 5

13. The circuit sketched below is called a relaxation oscillator.

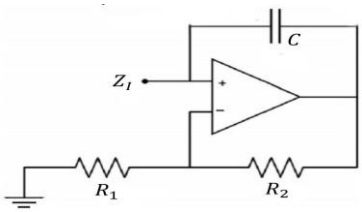


For the parameters indicated in the figure, the ratio of the maximum voltage at V_{out} to the maximum voltage at V_c is **[TIFR 2020]**

(a) 1/8 (b) 1/7

(c) 2/7 (d) 1/4

14. An operational amplifier is configured as shown in the figure below. For an AC input this circuit behaves effectively as **[TIFR 2021]**



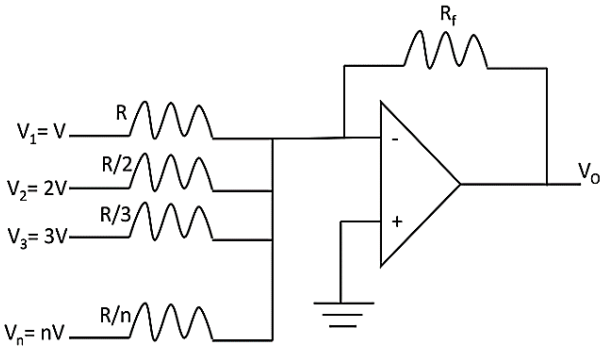
(a) a resistor with a negative resistance.

(b) an inductor with a negative inductance.

(c) a capacitor with a negative capacitance.

(d) an inductor with a positive inductance

15. Consider the following circuit with an op-amp.



If the output voltage V_0 is measured to be $V_0 = -V$, then the value of the feedback resistance R_f must be **[TIFR 2021]**

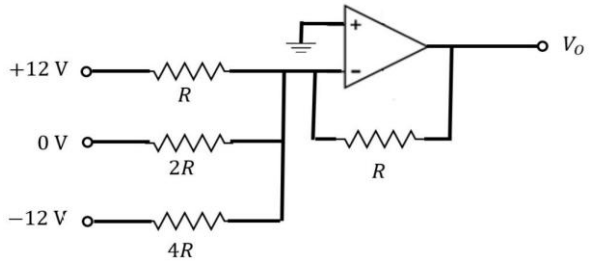
(a)$R_f = nR$

(b) $R_f = \dfrac{3R}{n(n+1)(2n+1)}$

(c) $R_f = \dfrac{6R}{n(n+1)(2n+1)}$

(d) $R_f = R/n$

16. Consider a circuit with an operational amplifier (op amp) and four resistors as sketched below.



The output voltage V_O is **[TIFR 2022]**

(a) -12 V (b) 0 V

(c) -9 V (d) -6 V

17. The non-inverting amplifier shown in the figure on the right is constructed using a nonideal operational amplified (op amp) with a finite open loop gain A.

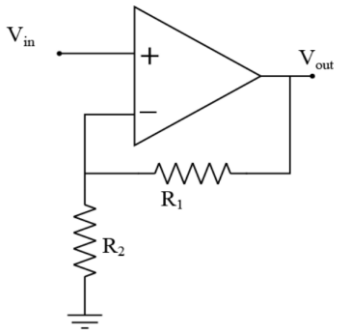
The value of feedback fraction is

$$B = \frac{R_2}{R_1 + R_2} = 0.1$$

If the gain A varies such that

$$10^4 < A < 10^5$$

then the approximate percentage variation in

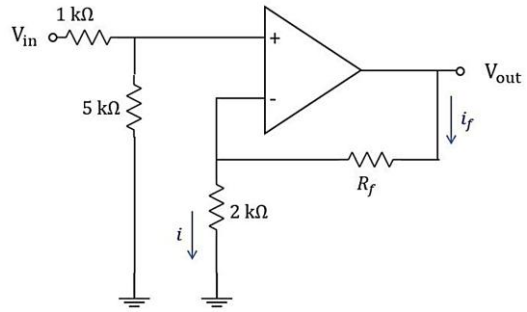


the closed loop gain will be. **[TIFR 2022]**

(a) 0.09% (b) 0.0%

(c) 0.9% (d) 9.0%

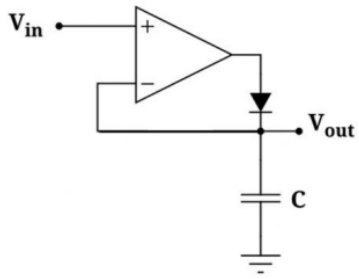
18. At what value of R_f will the ideal op-amp shown in the figure provide a gain of 6? **[TIFR 2023]**

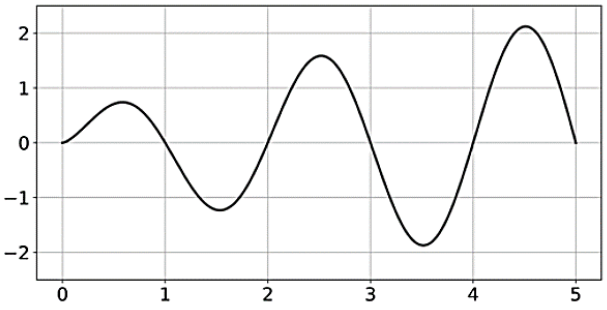


(a) 22.5kΩ (b) 19.5kΩ

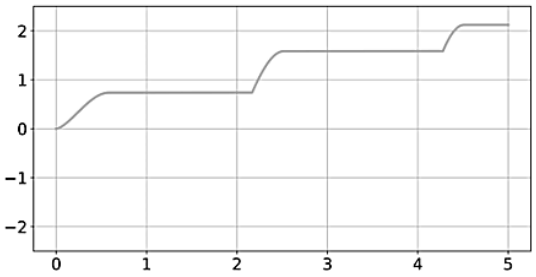
(c) 12.4kΩ (d) 14.4kΩ

19. For the circuit on the right, which graph represents V_{out} correctly for the V_{in} shown below? **[TIFR 2025]**

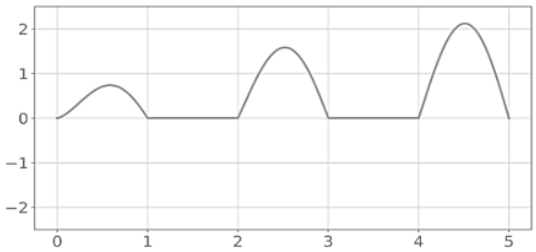




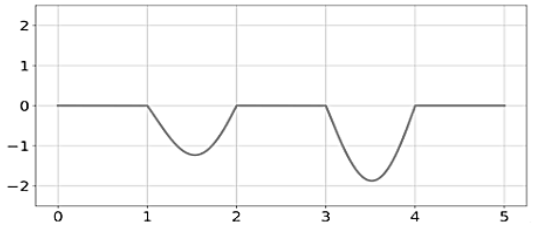
(a)



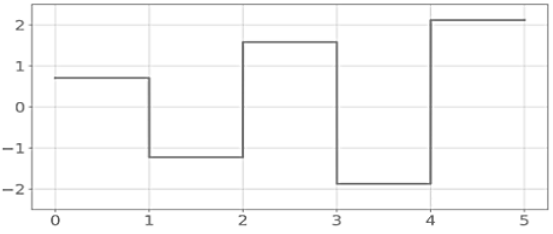
(b)



(c)



(d)



Answers key				
CSIR-NET				
1. a	2. a	3. c	4. d	5. b
6. c	7. b	8. a	9. a	10. c
11. c	12. c	13. d	14. d	15. b
16. c	17. b	18. a	19. a	20. d
21. a	22. a	23. d	24. c	25. a
26. a	27. d	28. b	29. b	
GATE				
1. c	2. d	3. a	4. d	5. d
6. a	7. b	8. c	9. d	10. b
11. c	12. a	13. a	14. d	15. a
16. b	17. a	18. b	19. b	20. c
21. 1	22. -3.6	23. c	24. c	25. acd
26. a	27. a	28. -12	29.	
JEST				
1. d	2. b	3. b	4. c	5. a
6. 5250	7. b	8. c	9. b	10. a
11. d				
TIFR				
1. b	2. c	3. a	4. d	5. c
6. c	7. c	8. b	9. a	10. b
11. b	12. a	13. a	14. c	15. c
16. c	17. c	18. c	19. a	

1. A resistance is measured by passing current through it and measuring the resulting voltage drop. If the voltmeter and the ammeter have uncertainties of 3% and 4%, respectively, then

(A) The uncertainty in the value of resistance is **[CSIR-JUNE 2011]**

(a) 7.0% (b) 3.5%

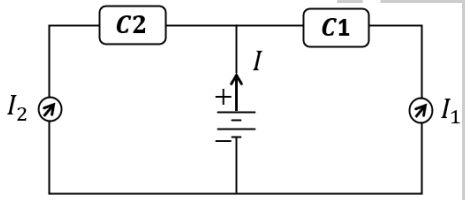
(c) 5.0% (d) 12.0%

(B) The uncertainty in the computed value of the power dissipated in resistance is

(a) 7% (b) 5%

(c) 11% (d) 9%

2. A battery powers two circuits C_1 and C_2 as shown in t the figure

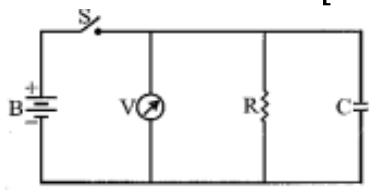


The total current I drawn from the battery is estimated by measuring the currents I_1 and I_2 through the individual circuits. If I_1 and I_2 are both 200 mA and if the errors in their measurement are 3 mA and 4 mA respectively, the error in the estimate of 1 is: **[CSIR-DEC 2011]**

(a) 7.0 mA (b) 7.5 Ma

(c) 5.0 mA (d) 10.5 mA

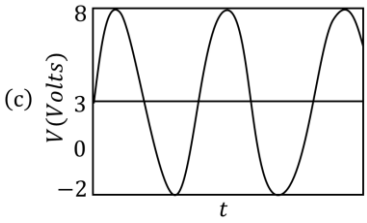
3. The insulation resistance R of an insulated cable is measured by connecting it in parallel with a capacitor C, a voltmeter, and battery B as shown. The voltage across the cable dropped from 150 V to 15 V, 1000 seconds after the switch S is closed. If the capacitance of the cable is 5μF then its insulation resistance is approximately **[CSIR-JUNE 2013]**



(a) $10^9\Omega$ (b) $10^8\Omega$

(c) $10^7\Omega$ (d) $10^6\Omega$

4. An ac signal of the type as shown in the figure, is applied across a resistor $R = 1\Omega$.

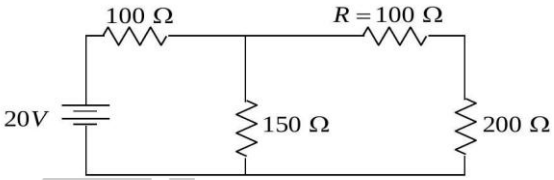


The power dissipated across the resistor is **[CSIR-JUNE 2019]**

(a) 12.5 W (b) 9 W

(c) 25 W (d) 21.5 W

5. Two voltmeters A and B with internal resistances $2M\Omega$ and 0.1kΩ are used to measure the voltage drops V_A and V_B, respectively, across the resistor R in the circuit shown below.



The ratio V_A/V_B is **[CSIR-JUNE 2020]**

(a) 0.58 (b) 1.73

(c) 1 (d) 2

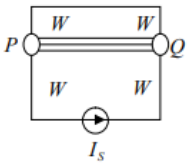
6. An inductor L, a capacitor C and a resistor R are connected in series to an AC source, $V = V_0 \sin \omega t$. If the net current is found to depend only on R, then **[CSIR-NOV 2020]**

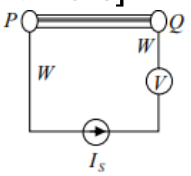
(a) $C = 0$ (b) $L = 0$

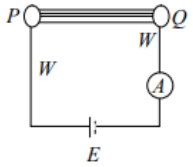
(c) $\omega = 1/\sqrt{LC}$ (d) $\omega = \sqrt{\frac{1}{LC} - \frac{R^2}{4L^2}}$

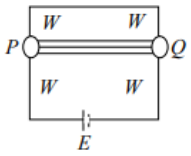
7. A circuit needs to be designed to measure the resistance R of a cylinder PQ to the best possible accuracy, using an ammeter A, a voltmeter V, a battery E and a current source I_S (all assumed to be ideal). The value of R is known to be approximately 10Ω, and the resistance W of each of the connecting wires is close to 10Ω. If the current from the current source and voltage from the battery are known exactly, which of the following circuits provides the most accurate measurement of R ?

[CSIR-JUNE 2023]

(a) 

(b) 

(c) 

(d) 

(a) B (b) A

(c) C (d) A

8. A train of impulses of frequency 500 Hz, in which the temporal width of each spike is negligible compared to its period, is used to sample a sinusoidal input signal of frequency 100 Hz. The sampled output is

[CSIR-JUNE 2023]

(a) Discrete with the spacing between the peaks being the same as the time period of the sampling signal

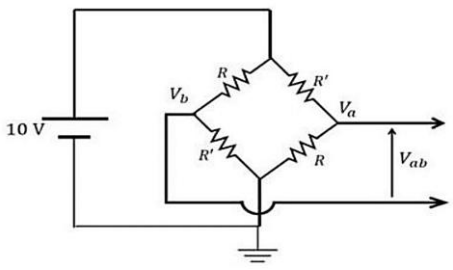
(b) a sinusoidal wave with the same time period as the sampling signal

(c) discrete with the spacing between the peaks being the same as the time period of the input signal

(d) a sinusoidal wave with the same time period as the input signal

9. In the circuit shown in the figure, the resistances R and R' change due to strain. While R increases, R' decreases by the same amount ΔR due to the applied strain. The unstrained values of R and R' are 100Ω each. If same strain is applied to all the resistors, and the output voltage (V_{ab}) changes to 0.3 V , then ΔR is closest to

[CSIR JUNE 2024]



(a)3Ω (b)1.5Ω

(c)4.5Ω (d)6Ω

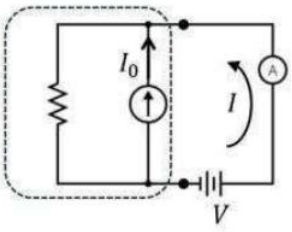
10. A battery with an open circuit voltage of 10 V is connected to a load resistor of 485Ω and the voltage measured across the battery terminals using an ideal voltmeter is 9.7 V . The internal resistance of the battery is closest to

[CSIR JUNE 2024]

(a)30Ω (b)15Ω

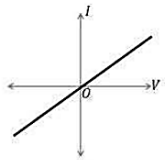
(c)20Ω (d)40Ω

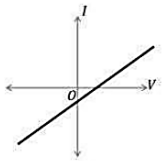
11. A circuit component consists of a resistor in parallel with an ideal current source. The $I-V$ characteristics of the component was measured using a variable voltage source and an ammeter 'A'.

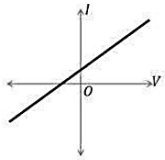


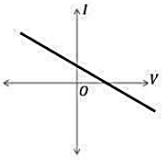
The arrow in the figure indicates the positive direction of current. The I-V characteristics of the component is best represented by

[CSIR DEC 2024]

1. 

2. 

3. 

4. 

❖ GATE PYQ

1. A resistance of 600Ω is parallel to an inductance of reactance 600(Ω) applied voltage, then the total impedance of the circuit is

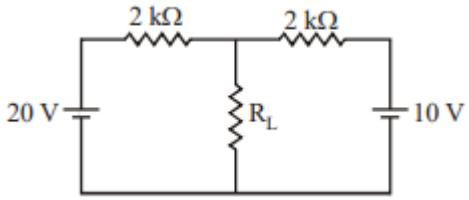
[GATE 2001]

(a) 628Ω (b) 268Ω

(c) 424Ω (d) 300Ω

2. In the circuit shown in the figure the Thevenin voltage V_{Th} and Thevenin resistance R_{Th} as

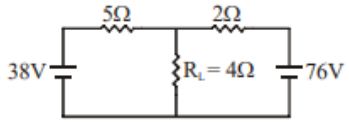
seen by the load resistance $R_L(=1k\Omega)$ are respectively **[GATE 2005]**



(a) 15 V, 1kΩ (b) 30 V, 4kΩ

(c) 20 V, 2kΩ (d) 10 V, 5Kω

3. For the circuit shown, the potential difference (in Volts) across R_L is **[GATE 2007]**



(a) 48 (b) 52

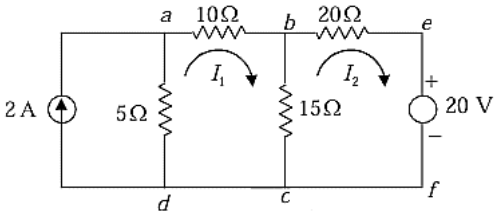
(c) 56 (d) 65

4. An a. c. voltage of 220 V_{ms} is applied to the primary of a 10:1 step-down transformer. The secondary of the transformer is centre lapped and connected to a full wave rectifier with a load resistance. The d. c. voltage appearing across the load is **[GATE 2008]**

(a) $\frac{22}{\pi}$ (b) $\frac{31}{\pi}$

(c) $\frac{62}{\pi}$ (d) $\frac{44}{\pi}$

5. Let I_1 and I_2 represent mesh currents in the loop abcda and befcb respectively. The correct expression describing Kirchoff's voltage loop law in one of the following loop is **[GATE 2008]**



(a) $30I_1 - 15I_2 = 10$

(b) $-15I_1 + 20I_2 = -20$

(c) $30I_1 - 15I_2 = -10$

(d) $-15I_1 + 20I_2 = 20$

6. For a given load resistance $R_L = 4.7$ohm, the power transfer efficiencies $\left(\eta = \frac{P_{load}}{P_{total}}\right)$ of a dc voltage source and a dc current source with internal resistances R_1 and R_2, respectively, are equal. The product R_1R_2 in units of ohm ^{2} (rounded off to one decimal place) is **[GATE 2019]**

7. A power supply has internal resistance R_S and open load voltage $V_S = 5$ V. When a load resistance R_L is connected to the power supply, a voltage drop of $V_L = 4V$ is measured across the load. The value of $\frac{R_L}{R_S}$ is (Round off to the nearest integer) **[GATE 2022]**

❖ JEST PYQ

1. The ratio of maximum to minimum resistance that can be obtained with $N1-\Omega$ resistors is **[JEST 2012]**

(a) N (b) N^2

(c) 1 (d) ∞

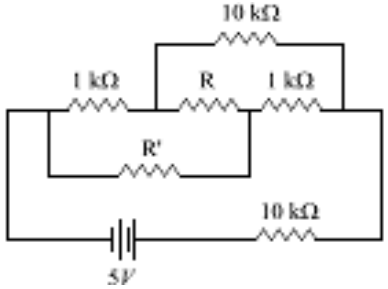
2. The temperature of a thin bulb filament (assuming that the resistance of the filament is nearly constant) of radius ' r ' and length L is proportional to **[JEST 2014]**

(a) $r^{1/4}L^{-1/2}$ (b) L^2r

(c) $r^{1/4}L^{-1}$ (d) r^2L^{-1}

3. It is found that when the resistance R indicated in the figure below is changed from $1k\Omega$ to $10k\Omega$, the current flowing through the resistance R' does not change. What is the value of the resistor R' ?

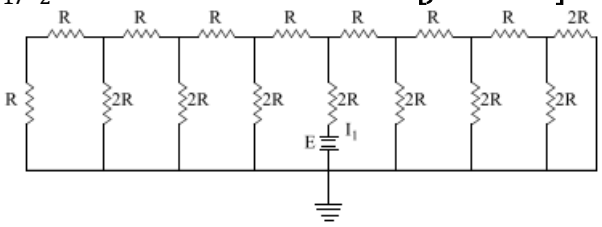
[JEST 2016]



(a) 5kΩ (b) 100Ω

(c) 10kΩ (d) 1Kω

4. For the circuit shown below, what is the ratio I_1/I_2 ? **[JEST 2017]**



Correct answer is (0016).

5. The ratio of maximum to minimum resistance that can be obtained with N number of $3-\Omega$ resistors is **[JEST 2020]**

(a) N (b) N^2

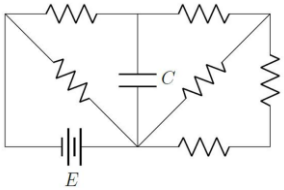
(c) N^3 (d) N^4

6. A carbon rod of resistance R_c and a metal rod of resistance R_m are connected in series. Let their linear temperature coefficients of resistivity have magnitudes α_c and α_m, respectively. The condition that the net resistance would be independent of temperature is **[JEST 2020]**

(a) $R_c = R_m$ (b) $\alpha_c = \alpha_m$

(c) $\frac{R_c}{R_m} = \frac{\alpha_m}{\alpha_c}$ (d) $\frac{R_m}{R_c} = \frac{\alpha_m}{\alpha_c}$

7. Consider the circuit shown in the figure below. C is the capacitance of the capacitor, E is the voltage provided by the battery and all the resistors are identical. What is the charge stored in the capacitor in units of CE, once it is fully charged. **[JEST 2023]**



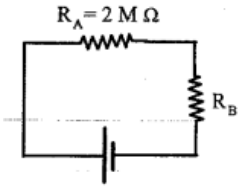
(a) $\frac{3}{4}$ (b) $\frac{5}{8}$

(c) $\frac{3}{8}$ (d) $\frac{5}{4}$

8. If a resistor of $10k\Omega$ and a capacitor of 0.5μ F are connected in series across an AC supply of 220 V (rms) at 50 Hz , what is the average power (in mW , to the nearest integer) dissipated in the circuit? **[JEST 2025]**

❖ TIFR PYQ

1. n the circuit given below, a person measures 9.0 V across the battery, 3.0 V across the 2MΩ resistor R_A and 4.5 V across the unknown resistor R_B, using an ordinary voltmeter which has a finite input resistance r. Assuming that the battery has negligible internal resistance, it follows that (i) the resistance R_B and (ii) the input resistance r of the voltmeter are, in MΩ, **[TIFR 2009]**



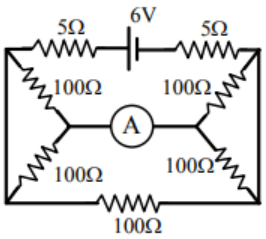
(a)$R_B = 3.0, r = 6.0$

(b) $R_B = 2.5, r = 7.5$

(c) $R_B = 4.0, r = 12.0$

(d) $R_B = 4.5, r = 10.0$

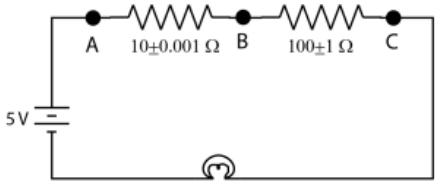
2. The current read by the ammeter (A) in the circuit given below is **[TIFR 2011]**



(a) 27.3 Ma (b) 100.0 mA

(c) 54.5 mA (d) 50.0 mA

3. You are given the following circuit and two instruments: a voltmeter and an ammeter both with 0.001% accuracy in their readings.



Which of the following methods will result in the most accurate reading for the current without interrupting the current in the circuit? **[TIFR 2014]**

(a) Use voltmeter to measure voltage across points B and C

(b) Use the ammeter to measure current at point B

(c) Use voltmeter to measure voltage across points A and B ☐

(d) Use voltmeter to measure voltage across points A and C

4. A student in the laboratory is provided with a bunch of standard resistors as well as the following instruments

----Voltmeter accurate to 0.1 V
---Thermometer accurate to 0.1C
----Ammeter accurate to 0.01 A
---Stop watch accurate to 0.05 s
----Constant current source (ideal)
---Constant voltage source (ideal)

Using this equipment (and nothing else), the student is expected to measure the resistance R of one of the given resistors. The least accurate result would be obtained by **[TIFR 2016]**

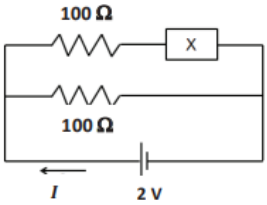
(a) measuring the Joule heating.

(b) passing a constant current and measuring the voltage across it.

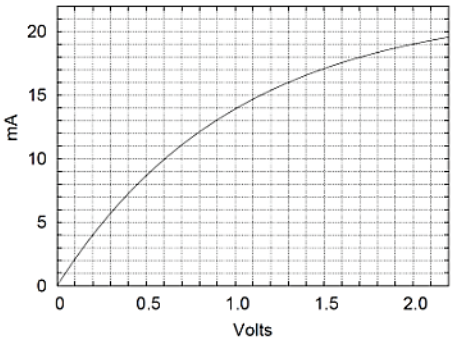
(c) measuring the current on application of a constant voltage across it.

(d) the Wheatstone bridge method.

5. The circuit shown below contains an unknown device X.

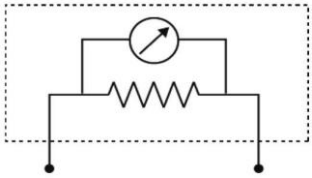


The current-voltage characteristics of the device X were determined and are shown in the plot given below. **[TIFR 2016]**



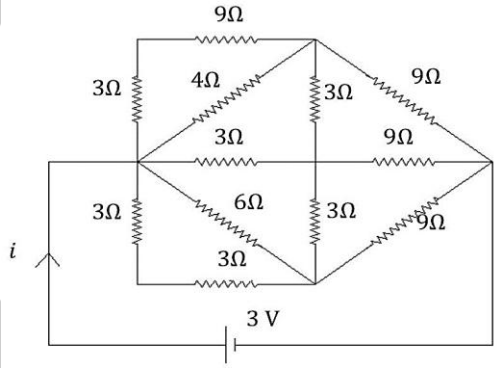
Determine the current I (in mA) flowing through the device X.

6. A realistic voltmeter can be modelled as an ideal voltmeter with an input resistor in parallel as shown below:



Such a realistic voltmeter, with input resistance 1kΩ, gives a reading of 100mV when connected to a voltage source with source resistance 50Ω. What will a similar voltmeter, with input resistance 1MΩ, read in mV, when connected to the same voltage source?] **[TIFR 2018]**

7. The current i flowing through the following circuit is

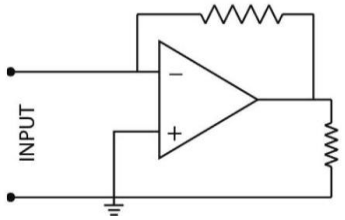


(a) 0.5 A (b) 0.6 A

(c) 0.75 A (d) 1.0 A

8. Consider the circuit shown on the right, which involves an op-amp and two resistors, with an input voltage marked INPUT.

Which of the following circuit components, when connected across the input terminals, is most likely to create a problem in the normal operation of the circuit? **[TIFR 2018]**



(a) A voltage source with very high Thevenin resistance.

(b) A current source with a very high Norton resistance.

(c) A voltage source with a very low Thevenin resistance.

(d) A current source with a very low Norton resistance.

9. A badly-designed voltmeter is modelled as an ideal voltmeter with a large resistor (R) and a large capacitor (C) connected in parallel to it. Given this information, which of the following statements describes what happens when this voltmeter is connected to a DC voltage source with voltage V and internal resistance $r (r \ll R)$? **[TIFR 2020]**

(a) The reading on the voltmeter rises slowly and becomes steady at a value slightly less than V.

(b) The reading on the voltmeter starts at a value slightly less than V and slowly falls to zero.

(c) The reading on the voltmeter rises slowly to a maximum value close to V and then slowly goes to zero.

(d) The reading on the voltmeter reads zero even when connected to the voltage source.

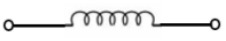
10. In an amplifier circuit, an input sine wave of amplitude 5 V gives a sine wave of amplitude 25 V as an output in an open load configuration. On applying a 20kΩ load resistance, the output drops to 10 V. This implies that the output resistance of the amplifier must be **[TIFR 2021]**

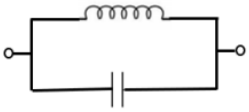
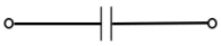
(a) 2kΩ (b) 20kΩ

(c) 10kΩ (d) 30kΩ

11. It is required to design a circuit with an impedance $Z(\omega)$ such that $Z(\omega) = ik(\omega - \omega_0)$ for a range of frequencies ω such that $|\omega - \omega_0|/\omega_0 \ll 1$ where k and ω_0 are constant real numbers.

A possible design for this circuit would correspond to

(a)  (b) 

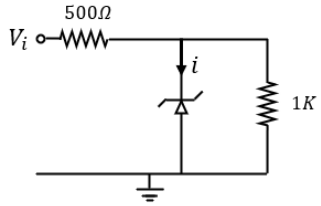
(c)  (d) 

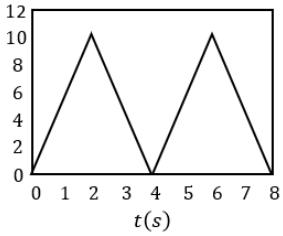
❖ **Answer Key**

CSIR-NET				
1. b/b	2. c	3. b	4. d	5. b
6. c	7. b	8. a	9. a	10. b
11. b				
GATE				
1. b	2. a	3. a	4. d	5. a
6. 22.09	7. 4			
JEST PYQ				
1. b	2. d	3. b	4. 0016	5. b
6. c	7. b	8. 3444		
TIFR PYQ				
1.	2.	3. c	4. a	5. 012
6. 105	7. c	8. c	9. a	10. d
11. a				

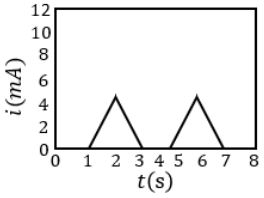
❖ CSIR-NET PYQ

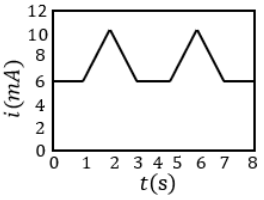
1. The figure below shows a voltage regulator utilizing a Zener diode of breakdown voltage 5 V and a positive triangular wave input of amplitude 10 V.

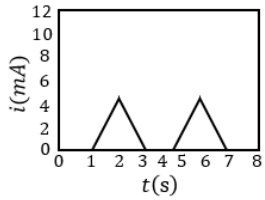


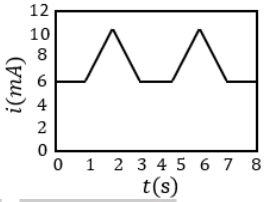


For $V_i > 5$ V, the Zener regulates the output voltage by channeling the excess current through it self. Which of the following waveforms shows the current ' i ' passing through the Zener diode? **[CSIR-DEC 2011]**

(a)


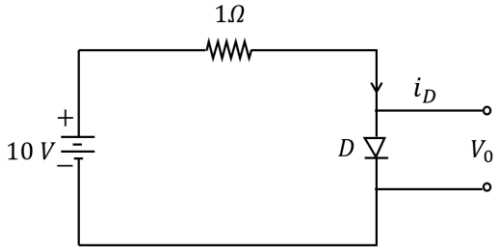
(b)


(c)


(d)


2. A diode D as shown in the circuit as an i $-$ v relation which can be proximated by

$$i_D = \begin{cases} v_D^2 + 2v_D, & \text{for } v_D > 0 \\ 0, & \text{for } v_D \le 0 \end{cases}$$



The value of v_D in the circuit is:

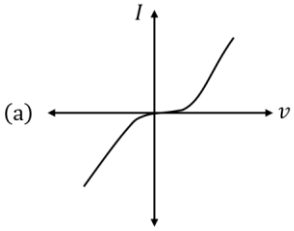
[CSIR-DEC 2012]

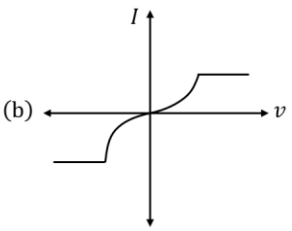
(a) $(-1+\sqrt{11})$V (b) 8 V

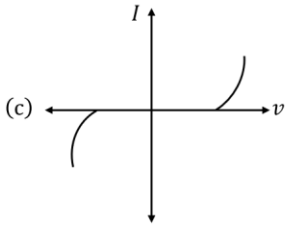
(c) 5 V (d) 2 V

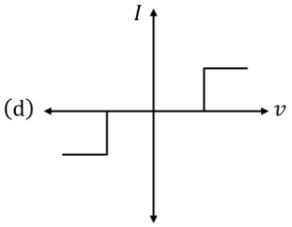
3. Two identical Zener diodes are placed back to back in series and are connected to a variable DC power supply. The best representation of the I-V characteristics of the circuit is

[CSIR-DEC 2013]

(a)


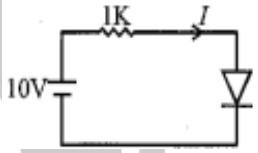
(b)


(c)


(d)


4. The $I-V$ characteristics of the diode in the circuit below is given by

$$I = \begin{cases} (V-0.7)/500 & \text{for } V \ge 0.7 \\ 0 & \text{for } V < 0.7 \end{cases}$$



where V is measured in volts and I is measured in amperes.

The current I in the circuit is

[CSIR-DEC 2014]

(a) 10.0 mA (b) 9.3 Ma

(c) 6.2 mA (d) 6.7 mA

5. Let I_0 be the saturation current, η the ideality factor and v_F and v_R the forward and reverse potentials, respectively, for a diode. The ratio R_R/R_F of its reverse and forward resistances R_R and R_F respectively, varies as (In the following k_B is the Boltzmani constant, T is the absolute temperature and q is the charge).

[CSIR-JUNE 2017]

(a) $\frac{v_R}{v_F}\exp\left(\frac{qv_F}{\eta k_B T}\right)$ (b) $\frac{v_F}{v_R}\exp\left(\frac{qv_F}{\eta k_B T}\right)$

(c) $\frac{v_R}{v_F}\exp\left(-\frac{qv_F}{\eta k_B T}\right)$ (d) $\frac{v_F}{v_R}\exp\left(-\frac{qv_F}{\eta k_B T}\right)$

6. A Zener diode with an operating voltage of 10 V at 25°C has a positive temperature co-efficient of 0.07% per °C of the operating voltage. The operating voltage of this Zener diode at 125°C is

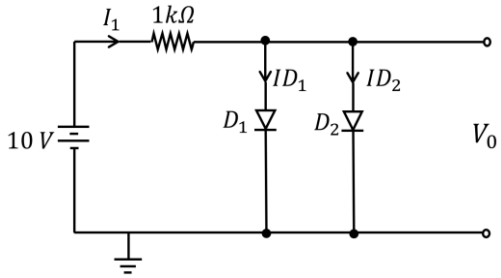
[CSIR-DEC 2017]

(a) 12.0 V (b) 11.7 V

(c) 10.7 V (d) 9.3 V

7. In the circuit below, D_1 and D_2 are two silicon diodes with the same characteristics. If the forward voltage drop of a silicon diode is 0.7 V, then the value of the current $I_1 + I_D$, is

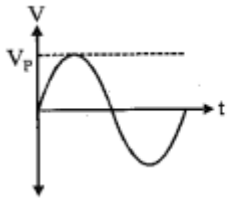
[CSIR-DEC 2017]

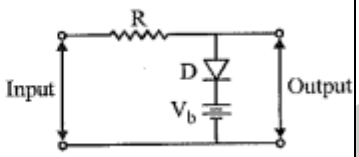


(a) 18.6 mA (b) 9.3 mA

(c) 13.95 mA (d) 14.65 Ma

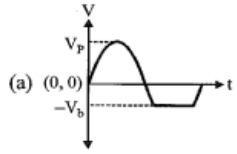
8. A sinusoidal voltage having a peak value of V_P is an input to the following circuit, in which the DC voltage is V_b.

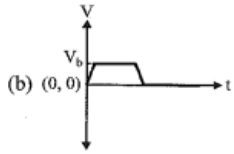


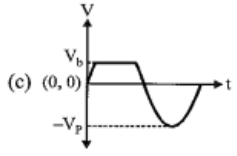


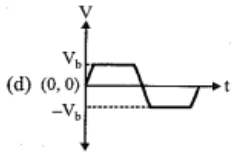
Assuming an ideal diode, which of the following best describes the output waveform?

[CSIR-DEC 2018]

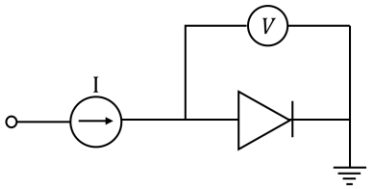








9. The forward diode current is given by $I = \kappa T^{\alpha} e^{-E_k/k_p T}(\exp(eV/k_B T) - 1)$, where E_g is the band gap of the semiconductor, V is the voltage drop across the diode, T is the temperature of the diode operating near room temperature and, α and κ are constants. A diode is used as a thermal sensor in the circuit shown below.



If V is measured using an ideal voltmeter to estimate T, the variation of the voltage V as a function of T is best approximated by (in the following a and b are constants)

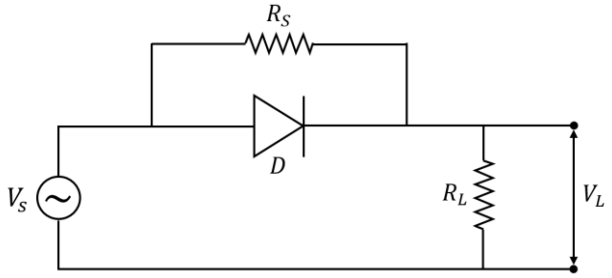
[CSIR-JUNE 2019]

(a) $aT^2 + b$ (b) $aT + b$

(c) $aT^3 + b$ (d) $aT + bT^2$

10. In the circuit below, D is an ideal diode, the source voltage $V_S = V_0 \sin\ \omega t$ is a unit amplitude sine wave and $R_S = R_L$.

[CSIR-DEC 2019]

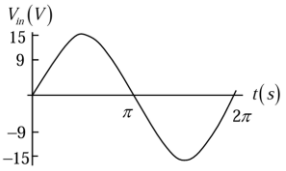


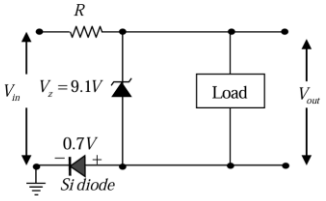
The average output voltage V_L, across the load resistor R_L is

(a) $\frac{1}{2\pi}V_0$ (b) $\frac{3}{2\pi}V_0$

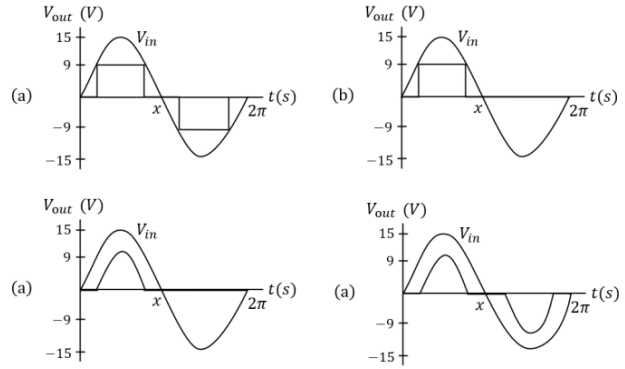
(c) $3V_0$ (d) V_0

11. A high impedance load network is connected in the circuit as shown below

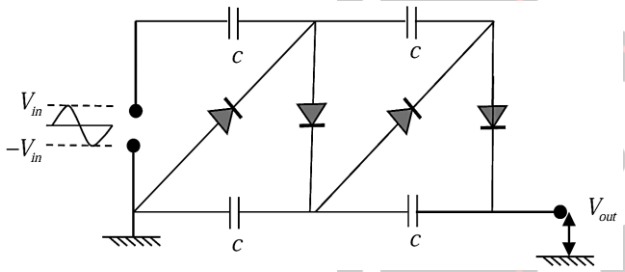




The forward voltage drop for silicon diode is 0.7 V and the Zener voltage is 9.10 V. If the input voltage (V_{in}) is sine wave with an amplitude of 15 V (as shown in the figure above), which of the following waveform qualitatively describes the output voltage (V_{out}) across the load? **[CSIR-JUNE 2022]**



12. In the circuit shown below, four silicon diodes and four capacitors are connected to a sinusoidal voltage source of amplitude $V_{\text{in}} > 0.7$ V and frequency 1kHz. If the knee voltage for each of the diodes is 0.7 V and the resistances of the capacitors are negligible, the DC output voltage V_{out} after 2 seconds of starting the voltage source is closest to **[CSIR-JUNE 2023]**

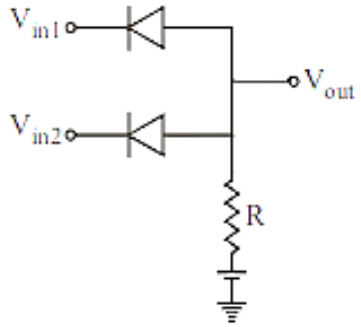


(a) $4V_{\text{in}} - 0.7V$ (b) $4V_{\text{in}} - 2.8$ V

(c) $V_{\text{in}} - 0.7$ V (d) $V_{\text{in}} - 2.8$ V

❖ GATE PYQ

1. The circuit shown can be used as **[GATE 2005]**

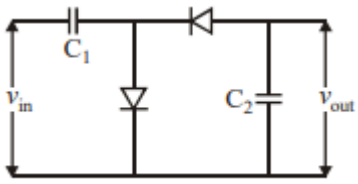


(a) NOR gate (b) OR gate

(c) NAND gate (d) AND gate

2. A sinusoidal input voltage v_{in} of frequency ω is fed to the circuit shown in the figure, where $C_1 \gg C_2$. If v_m is the peak value of the input voltage, then output voltage (v_{out}) is

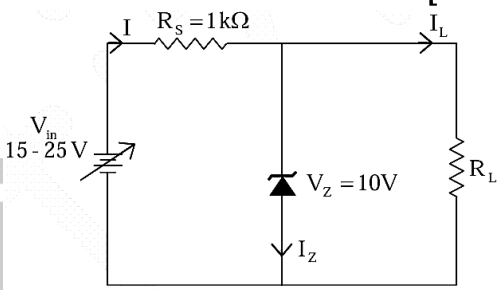
[GATE 2006]



(a) $2v_m$ (b) $2v_0 \sin\ \omega t$

(c) $\sqrt{2}v_m$ (d) $\frac{v_m}{2} \sin\ \omega t$

3. Pick the correct statement based on the above circuit **[GATE 2009]**



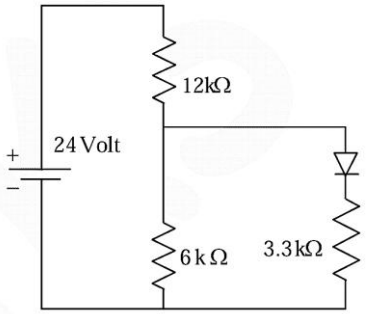
(a) The maximum Zener current, $I_{z(\max)}$ when $R_L = 10\text{k}\Omega$ is 15 mA

(b) The minimum Zener current, $I_{z(\min)}$, when $R_L = 10k\Omega$ is 5 mA

(c) With $V_{\text{in}} = 20$ V, $I_L = I_Z$ when $R_L = 2k\Omega$

(d) The power dissipated across the Zener when $R_L = 10\text{k}\Omega$ and $V_{\text{in}} = 20$ V is 100 mW

4. In the following circuit, the voltage drop across the ideal diode in forward bias conditions is 0.7 V **[GATE 2012]**



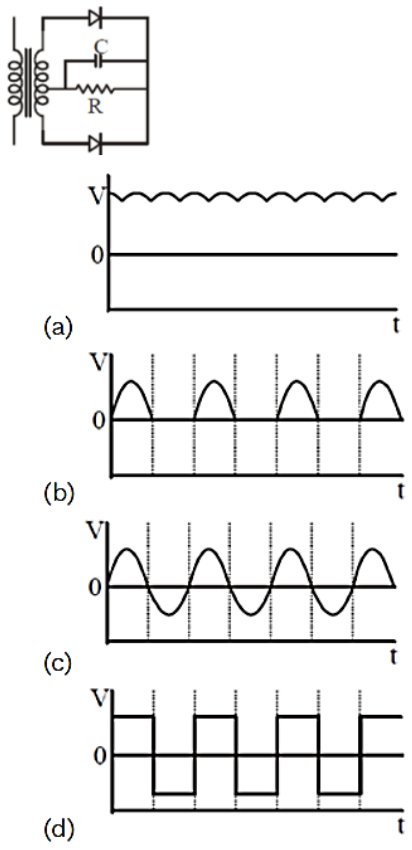
The current passing through the diode is

(a) 0.5 mA (b) 1.0 mA

(c) 1.5 mA (d) 2.0 Ma

5. In the figure given below, the input to the primary of the transformer is a voltage varying sinusoidally with time. The resistor R is

connected to the centre tap of the secondary. Which one of the following plots represents the voltage across the resistor R as a function of time? **[GATE 2012]**



6. Consider the circuit given in the figure. Let the forward voltage drop across each diode be 0.7 V. The current I (in mA) through the resistor is **[GATE 2020]**

7. Choose the most appropriate matching of the items in Column 1 with those in Column 2. **[GATE 2023]**

Column 1	Column 2
(i) PIN diode	P. Voltage regulation
(ii) Tunnel diode	Q. Radio frequency and microwave devices
(iii) Zener diode	R. Optoelectronic detection
(iv) Photo diode	S. Oscillator

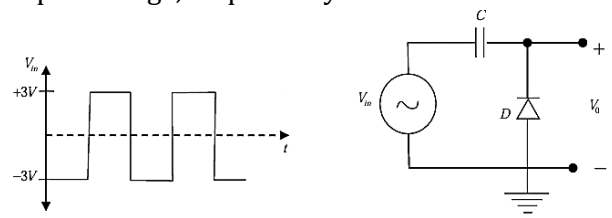
(a) (i) - Q; (ii) - S; (iii) - P; (iv) - R

(b) (i) - R; (ii) - Q; (iii) - P; (iv) – S

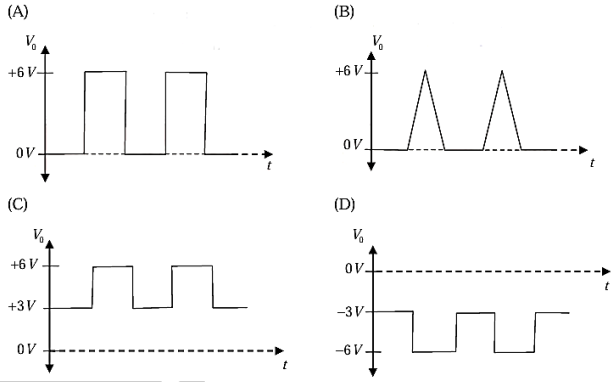
(c) (i) - R; (ii) - S; (iii) - P; (iv) - Q

(d) (i) - P; (ii) - Q; (iii) - R; (iv) – S

8. The symbols C, D, V_{in} and V_0 shown in the figure denote capacitor, ideal diode, input voltage and output voltage, respectively.

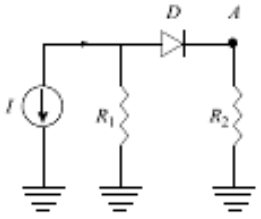


Which one of the following output waveforms (V_0) is correct for the given input waveform (V_{in})? **[GATE 2024]**



❖ JEST PYQ

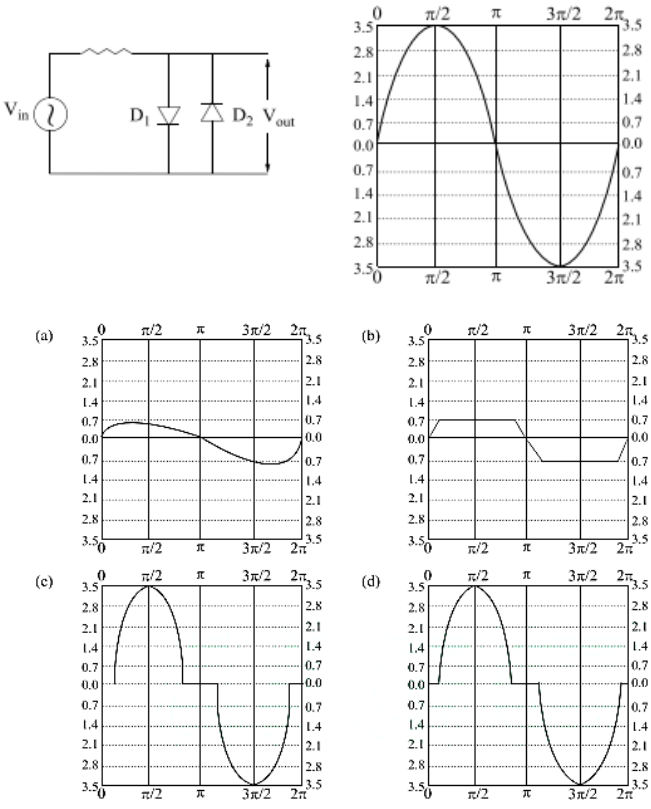
1. Consider the circuit shown in the figure where $R_1 = 2.07\text{k}\Omega$ and $R_2 = 1.93\text{k}\Omega$ current source I delivers 10 mA current. The potential across the diode D is 0.7 V. What is the potential at A? **[JEST 2017]**



(a) 10.35 V (b) 9.65 V

(c) 19.30 V (d) 4.83 V

2. In the following silicon diode circuit ($V_B = 0.7$ V), determine the output waveform (V_{out}) for the given input wave. **[JEST 2017]**



3. A Germanium diode is operated at a temperature of 27 degree C. the diode terminal voltage is 0.3 V when the forward current is 10 mA. What is the forward current (in mA) if the terminal voltage is 0.4 V ?

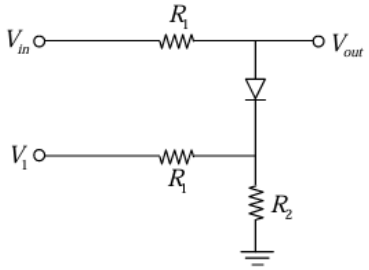
[JEST 2018]

(a) 477.3 (b) 577.3

(c) 47.73 (d) 57.73

4. The circuit given below is fed by a sinusoidal voltage $V_{\text{in}} = V_0 \sin\ \omega t$. Assume that the cut-in voltage of the diode is 0.7 volts and V_1 is a positive dc voltage smaller than V_0. Which one of the following statements is true about V_{out} ?

[JEST 2019]



(a) Positive part of V_{out} is restricted to a maximum voltage of $0.7 + \frac{R_2}{R_1+R_2}V_1$

(b) Negative part of V_{out} is restricted to a maximum voltage of $0.7 + \frac{R_2}{R_1+R_2}V_1$

(c) Positive part of V_{out} is restricted to a maximum voltage of $0.7 + \frac{R_1}{R_1+R_2}V_1$

(d) Negative part of V_{out} is restricted to a maximum voltage of $0.7 + \frac{R_1}{R_1+R_2}V_1$

5. In an open circuited $p-n$ junction diode, the barrier voltage at the junction is generated due to **[JEST 2021]**

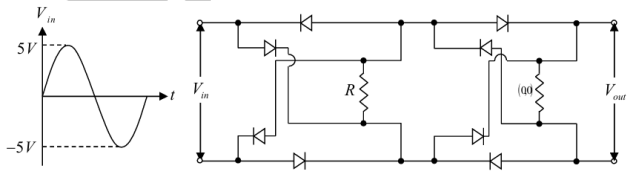
(a) Minority carriers in the p and n sides

(b) Majority carriers in the p and n sides

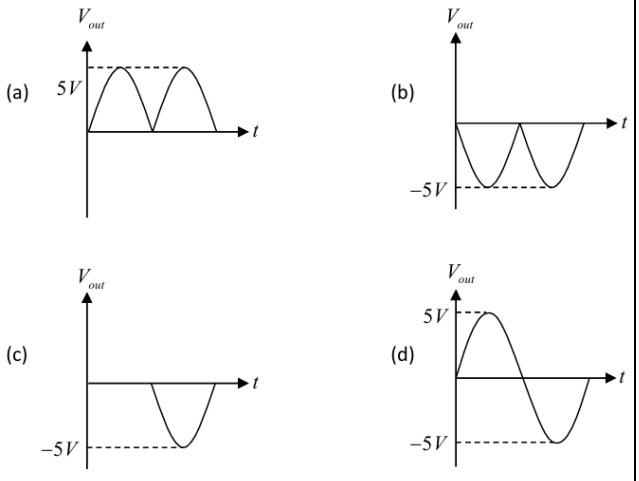
(c) Immobile negative charge in the p-side and positive charge in the n-side

(d) Immobile positive charge in the p-side and negative charge in the n-side

6. The circuit given in the figure below is composed of ideal diodes and resistances R. The input waveform is shown on the left.

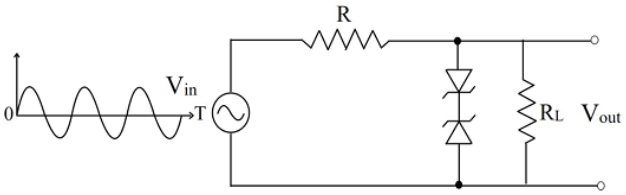


The output waveform would be **[JEST 2021]**



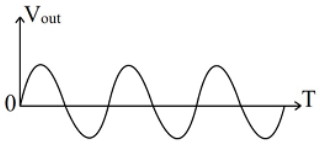
7. What is the output waveform of the circuit for the given input signal? Assume that the zener diodes are identical, amplitude of the input voltage V_{in} is twice the zener breakdown voltage, and $R_L = 10R$.

[JEST 2024]



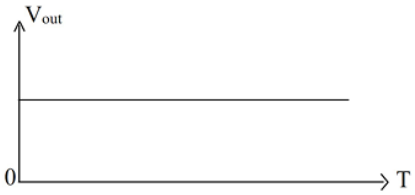
A.

B.



C.

D.



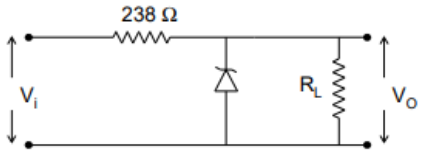
8. A silicon p-n junction diode operates at 27°C. The current I is doubled when the forward bias is increased. The increase in the forward bias is closest to:
[Assume $I \gg I_s$, where I_s is the reverse saturation current and the emission coefficient $\eta_{Si} = 2$.] **[JEST 2025]**

(a) 54 mV (b) 36 mV

(c) 72 mV (d) 18 mV

❖ TIFR PYQ

1. The voltage regulator circuit shown in the figure has been made with a Zener diode rated at 15 V, 200 mW. It is required that the circuit should dissipate 150 mW power across the fixed load resistor R_L. **[TIFR 2012]**



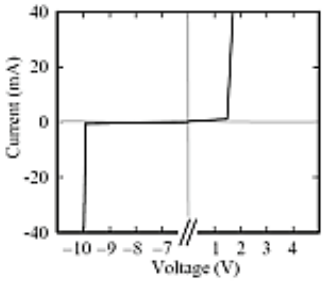
For stable operation of this circuit, the input voltage V_i must have a range

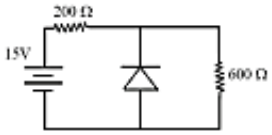
(a) 17.5 V – 20.5 V (b) 15.5 V – 20.5 V

(c) 15.5 V – 22.5 V (d) 17.5 V – 22.5 V

(e) 15.0 V – 22.5 V

2. The figure on the right shows the current voltage characteristics of a diode over a range of voltage and current where it is safe to operate the diode. **[TIFR 2013]**



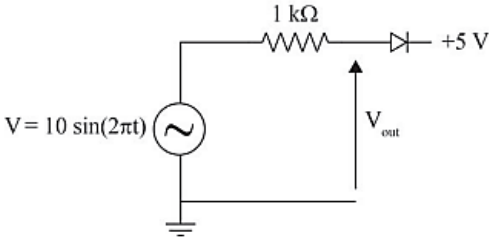


When this diode is used in the circuit on the extreme right, the approximate current, in mA , through the diode will be

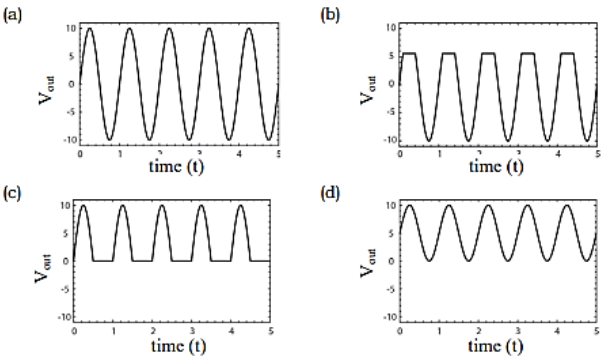
(a) 0 (b) 8.3

(c) 16.7 (d) 25

3. Consider the following circuit.

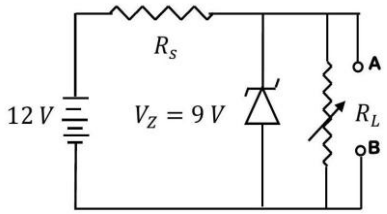


Which of the graphs given below is a correct representation of V_{out} ? **[TIFR 2014]**



4. Drawing power from a 12 V car battery, a 9 V stabilized DC voltage is required to power a car stereo system, attached to the terminals A and B, as shown in the figure.

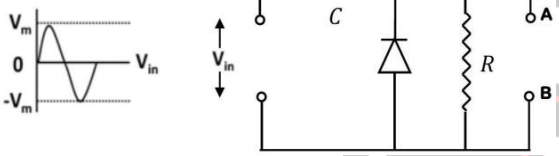
If a Zener diode with ratings, $V_z = 9$ V and $P_{max} = 0.27$ W, is connected as shown in the figure, for the above purpose, the minimum series resistance R_S must be **[TIFR 2019]**



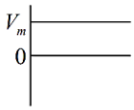
(a) 111Ω (b) 103Ω

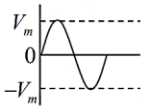
(c) 100Ω (d) 97Ω

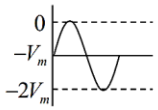
5. The signal shown on the left side of the figure below is fed into the circuit shown on the right side.

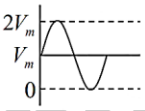


If the signal has time period τ_S and the circuit has a natural frequency τ_{RC}, then, in the case when $\tau_S \ll \tau_{RC}$, the steady-state output will resemble **[TIFR 2019]**

(a) 

(b) 

(c) 

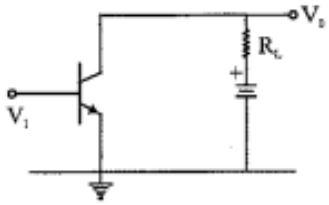
(d) 

❖ Answer Key				
CSIR-NET				
1. a	2. d	3. c	4. c	5. b
6. c	7. c	8. c	9. b	10. a
11. d	12. b			
GATE				
1. d	2. a	3. c	4. b	5. a
6. 8	7. a	8. 8		
JEST				
1. b	2. b	3. a	4. a	5. c
6. a	7. a	8. b		
TIFR PYQ				
1. a	2. b	3. b	4. c	5. d

Bipolar Junction Transistor

❖ CSIR-NET PYQ

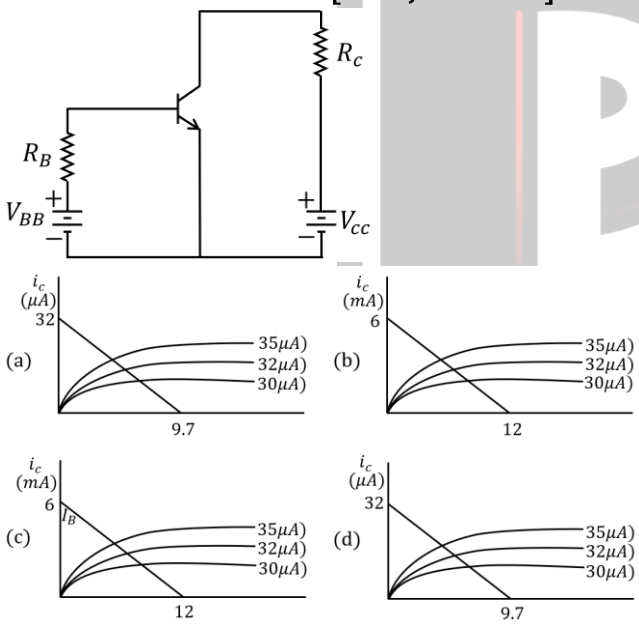
1. The transistor in the given circuit has $h_{fc} = 35\Omega$ and $h_{ie} = 1000\Omega$. If the load resistance $R_L = 1000\Omega$, the voltage and current gain are, respectively. **[CSIR-JUNE 2012]**



(a) $-35, -35$ (b) $35, -35$

(c) $35, -0.97$ (d) $0.98, -35$

2. A silicon transistor with built-in voltage 0.7 V is used in the circuit shown, with $V_{BB} = 9.7$ V, $R_B = 300\text{k}\Omega$, $V_{CC} = 12$ V and $R_C = 2\text{k}\Omega$. Which of the following figures correctly represents the load line and the quiescent Q point? **[CSIR-JUNE 2013]**



3. A large MOS transistor consists of N individual transistors connected in parallel. If the only form of noise in each transistor is $1/f$ noise, then the equivalent voltage noise spectral density for the MOS transistor is **[CSIR-DEC 2014]**

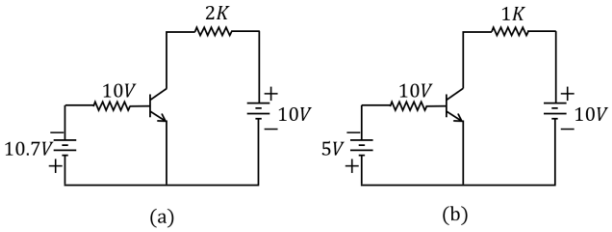
(a) $1/N$ times that of a single transistor

(b) $1/N^2$ times that of a single transistor

(c) N times that of a single transistor

(d) N^2 times that of a single transistor

4. Consider the circuits shown in Figures (a) and (b) below.



If the transistors in Figures (a) and (b) have current gain (β_{tik}) of 100 and 10 respectively, then they operate in the **[CSIR-JUNE 2015]**

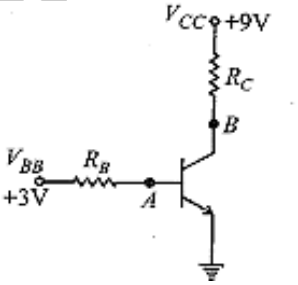
(a) active region and saturation region respectively

(b) saturation region and active region respectively

(c) saturation region in both cases

(d) active region in both cases

5. In the circuit below the voltages V_{BB} and V_{CC} are kept fixed, the voltage measured at B is a constant, but that measured at A fluctuates between a few μV to a few mV.



From these measurements it may be inferred that the **[CSIR-DEC 2017]**

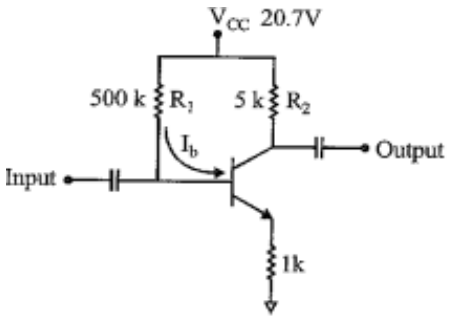
(a) base is open internally

(b) emitter is open internally

(c) collector resistor is open

(d) base resistor is open

6. In the following circuit, the value of the common-emitter forward current amplification factor β for the transistor is 100 and V_{BE} is 0.7 V.

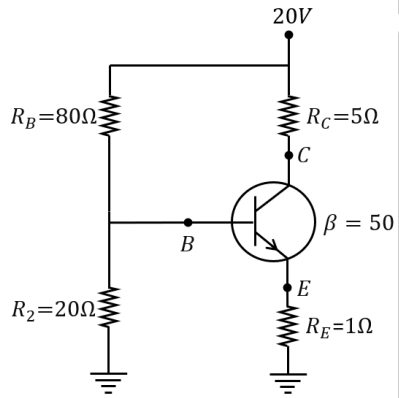


The base current I_B is **[CSIR-JUNE 2018]**

(a) 40μA (b) 30μA

(c) 44μA (d) 33μA

7. An *npn*-transistor is connected in a voltage divider configuration as shown in the figure below



If the resistor R_2 is disconneted, the voltages V_B at the base and V_c at the collector change as follows. **[CSIR-JUNE 2019]**

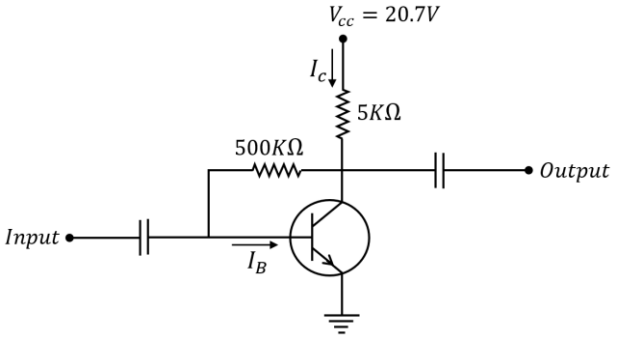
(a) Both V_B and V_C increase

(b) Both V_B and V_C decrease

(c) V_B decreases, but V_C increase

(d) V_B increases, but V_C decreases

8. In a collector feedback circuit shown in the figure below, the base emitter voltage $V_{BE} = 0.7$ V and current gain $\beta = \frac{I_C}{I_B} = 100$ for the transistor

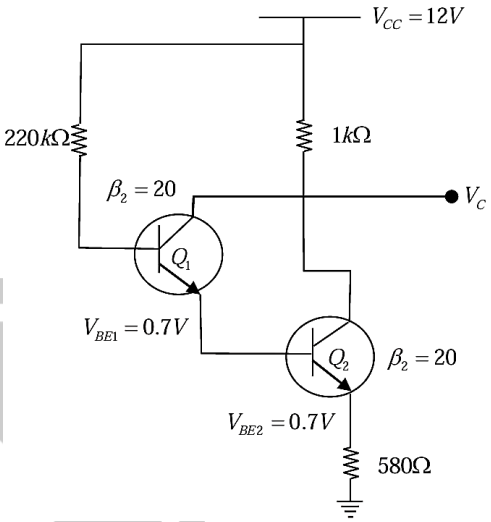


The value of the base current I_B is **[CSIR-DEC 2019]**

(a) 20μA (b) 40μA

(c) 10μA (d) 100μA

9. The figure below shows a circuit with two transistors, Q_1 and Q_2, having current gains β_1 and β_2 respectively.



The collector voltage V_C will be closest to **[CSIR-JUNE 2022]**

(a)0.9 V (b)2.2 V

(c)2.9 V (d)4.2 V

10. An amplifier with a voltage gain of 40 dB without feedback is used in an electronic circuit. A negative feedback with a fraction 1/40 is connected to the input of this amplifier. The net gain of the amplifier in the circuit is closest to **[CSIR-JUNE 2022]**

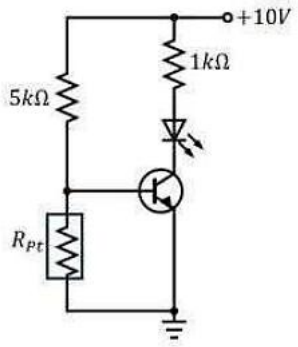
(a)40 dB (b)37 dB

(c)29 dB (d)20 Db

11. An LED is required to glow brightly when the temperature sensed by a Platinum resistance thermometer exceeds a certain value. In the circuit shown below, the resistance of the Pt thermometer (in ohms) varies as

$$R_{Pt}(T) = 100 + 0.4\,T$$

where T is temperature in degree Celsius. The transistor turns on when $V_{BE} > 0.7$ V and it has a very high current gain. The temperature at which the LED would start glowing is closest to **[CSIR DEC 2024]**



(a)850°C (b)400°C

(c)500°C (d)700°C

❖ GATE PYQ

1. In an $n-p-n$ transistor, the leakage current consists of **[GATE 2001]**

(a) electrons moving from the base to the emitter

(b) electrons moving from the collector to the base

(c) electrons moving from the collector to the emitter

(d) electrons moving from the base to the collector

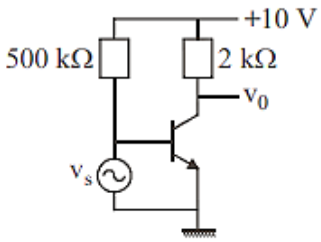
2. A bipolar junction transistor with one junction forward biased and either the collector or emitter open, operates in the **[GATE 2004]**

(a) cut-offregion (b) saturation region

(c) pinch-offregion (d) active region

3. Figure shows a common emitter amplifier with $\beta = 100$. What is the maximum peak to peak input signal (v_s) for which is distortion-free output may be obtained? **[GATE 2004]**

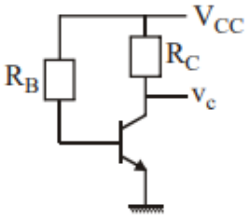
[Assume $V_{BE} = 0$ and $r_e = 20\Omega$]



(a) 40mV (b) 60Mv

(c) 80mV (d) 100mV

4. Calculate the collector voltage (v_c) of the transistor circuit is shown in the figure. [Given: $\alpha = 0.96, I_{CB0} = 20\mu A, V_{BE} = 0.3$ V, $R_B = 100$kΩ, $V_{CC} = +10$ V and $R_C = 2.2$kΩ] **[GATE 2004]**



(a) 3.78 V (b) 3.82 V

(c) 4.72 V (d) 9.7 V

5. A power amplifier gives 150 W output for an input of 1.5 W. The gain, in dB, is **[GATE 2007]**

(a) 10 (b) 20

(c) 54 (d) 100

6. In a typical npn transistor the doping concentrations in emitter, base and collector regions are C_E, C_B and C_C respectively. These satisfy the relation **[GATE 2007]**

(a) $C_E > C_C > C_B$ (b) $C_E > C_B > C_C$

(c) $C_C > C_B > C_E$ (d) $C_E = C_C > C_B$

7. A common emitter transistor amplifier circuit is operated under a fixed bias. In this circuit, the operating point **[GATE 2008]**

(a) remains fixed with an increase in temperature

(b) moves towards cut-off region with an increase in temperature

(c) moves towards the saturation region with a decrease in temperature

(d) moves towards the saturation region with an increase in temperature

8. An amplifier of gain 1000 is made into a feedback amplifier by feeding 9.9% of its output voltage in series with the input opposing. If $f_L =$ 20 Hz and $f_H = 200$kHz for the amplifier without feedback, then due to the feedback **[GATE 2009]**

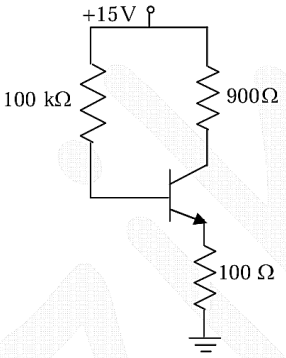
(a) the gain decreases by 10 times

(b) the output resistance increases by 10 times

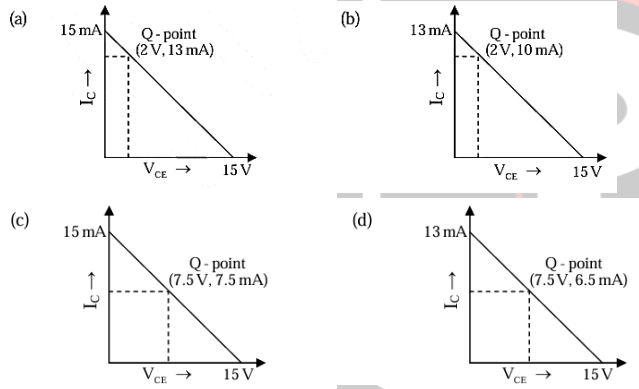
(c) the f_H increases by 100 times

(d) the input resistance decreases by 100 times

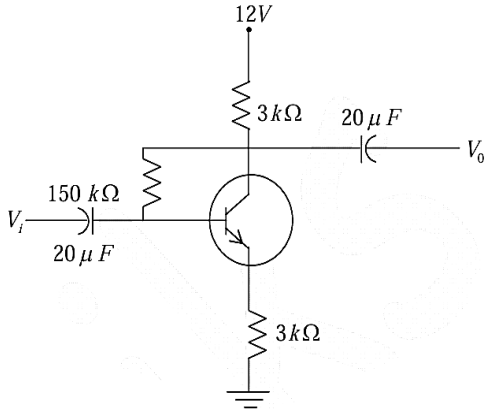
9. Consider the following circuit in which the current gain β_{dc} lof the transistor is 100



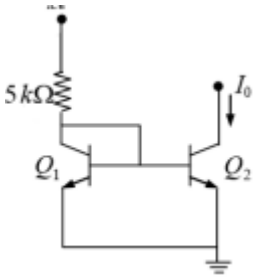
Which one of the following correctly represent the load line (collector current I_C with respect to collector emitter voltage V_{CE}) and Q-point of this circuit? **[GATE 2012]**



10. The current gain of the transistor in the following circuit is $\beta_{dc} = 100$. The value of collector current I_C is **[GATE 2014]**

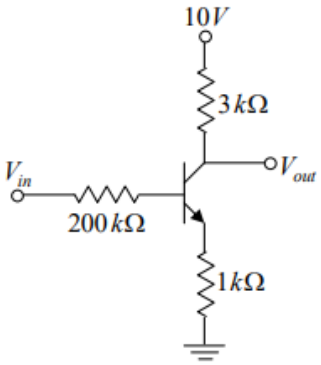


11. In the simple current source shown in the figure, Q_1 and Q_2 are identical transistors with current gain $\beta = 100$ and $V_{BE} = 0.7$ V



The current I_0 (in mA)_____ is (upto two decimal places) **[GATE 2015]**

12. For the transistor shown in the figure, assume $V_{BE} = 0.7$ V and $\beta_{dc} = 100$. If $V_{\text{in}} = 5$ V, V_{out} (in Volts) is____ (Give your answer upto one decimal place) **[GATE 2016]**

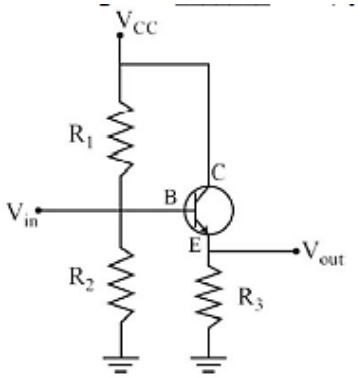


13. For the transistor amplifier circuit shown below with $R_1 = 10k\Omega, R_2 = 10k\Omega, R_3 = 1k\Omega$ and $\beta = 99$. Neglecting the emitter diode resistance, the input impedance of the amplifier looking into the base for small ac signal is kΩ. (up to two decimal places)

[GATE 2017]

14. For a bipolar junction transistor, which of the following statements are true? **[GATE 2022]**

(a) Doping concentration of emitter region is more than that in collector and base region



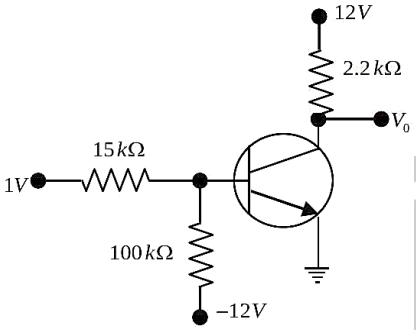
(b) Only electrons participate in current conduction

(c) The current gain β depends on temperature

(d) Collector current is less than the emitter current

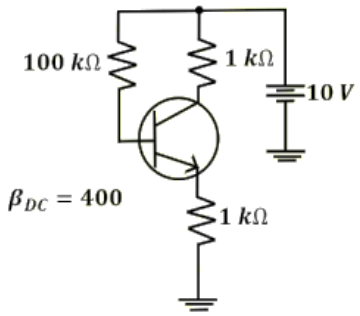
15. For a transistor amplifier, the frequency response is such that the mid band voltage gain is 200. The cutoff frequencies are 20 Hz and 20kHz. What is the ratio (rounded off to two decimal places) of the voltage gain at 10 Hz to that at 100kHz ? **[GATE 2023]**

16. A typical biasing of a silicon transistor is shown in figure.



The value of common-emitter current gain β for the transistor is 100 . Ignore reverse saturation current. The output voltage V_0 (in V) is (in integer). **[GATE 2024]**

17. In the transistor circuit shown in the figure, $V_{BE} = 0.7$ V and $\beta_{DC} = 400$. The value of the base current in μA (rounded off to one decimal place) is



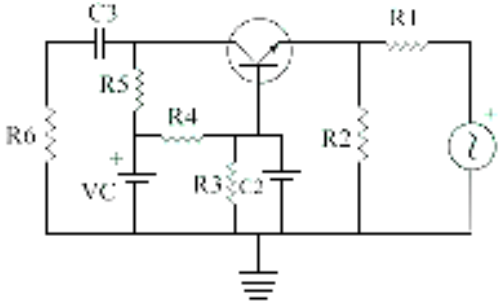
❖ JEST PYQ

1. A transistor in common base configuration has ratio of collector current to emitter current β and ratio of Collector to base current α. Which of the following is true? **[JEST 2016]**

(a) $\beta = \dfrac{\alpha}{(\alpha+1)}$ (b) $\beta = \dfrac{(\alpha+1)}{\alpha}$

(c) $\beta = \dfrac{\alpha}{(\alpha-1)}$ (d) $\beta = \dfrac{(\alpha-1)}{\alpha}$

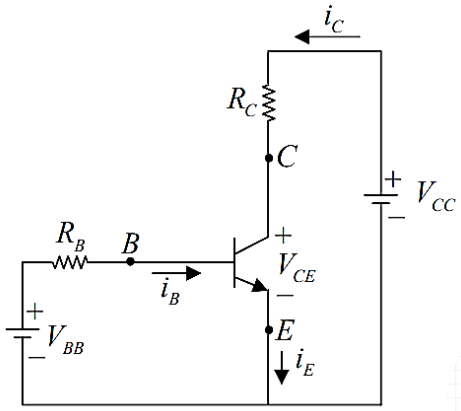
2. What is the DC base current (approximated to nearest integer value in μA) for the following $n-p-n$ silicon transistor circuit, given $R_1 = 75\Omega, R_2 = 4.0\text{k}\Omega, R_3 = 2.1\text{k}\Omega, R_4 = 2.6\text{k}\Omega, R_5 = 6.0\text{k}\Omega, R_6 = 6.8\text{k}\Omega, C_1 = 1\mu F, C_2 = 2\mu F$, $V_C = 15V$ and $\beta_{dc} = 75$? **[JEST 2017]**



(a) 20 (b) 24

(c) 16 (d) 35

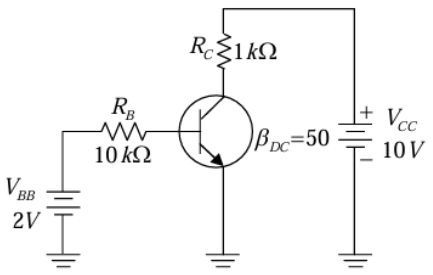
3. Consider the transistor circuit shown in the figure. Assume $V_{BEQ} = 0.7$ V, $V_{BB} = 6$ V



And the leakage current is negligible. What is the required value of R_B in kilo-ohms if the base current is to be 4μA ?

[JEST 2018]

4. Calculate the collector current and determine whether or not the transistor in figure shown below is in saturation. Assume V_{CE} (sat) = 0.2 V **[JEST 2020]**



(a)6.5 mA, not in saturation

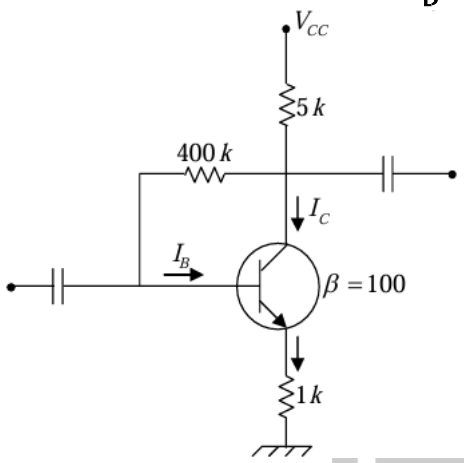
(b) 11.5 mA, in saturation

(c) 11.5 mA, not in saturation

(d) 6.5 mA, in saturation

5. Analyze the common emitter transistor circuit given in the figure. If the current gain (β) increases by 50%, the relative change in collector current (I_C) is approximately

[JEST 2020]



(a) 5%

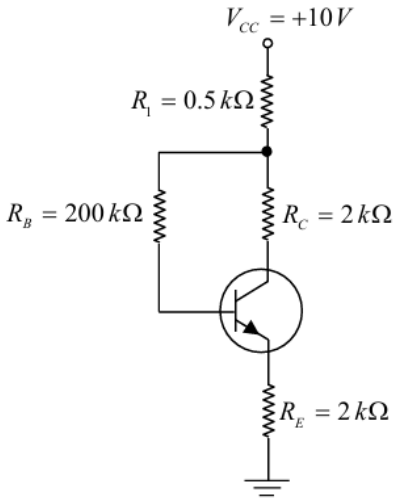
(b) 15%

(c) 20%

(d) 25%

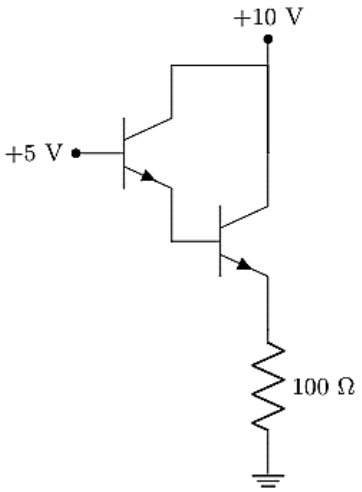
6. In the following transistor circuit $R_1 = 0.5\text{k}\Omega, R_E = R_C = 2\text{k}\Omega, R_B = 200\text{k}\Omega, \beta = \frac{I_C}{I_B} = 100, V_{CC} = 10\text{ V}, V_{BE} = 0.7\text{ V}$. Determine the V_{CE} in mV.

[JEST 2021]



7. The base current in the first transistor of the following circuit having two identical Silicon-based *npn* transistors of β value 100, is closest to

[JEST 2022]



(a) 5.0 Ma

(b) 0.36 mA

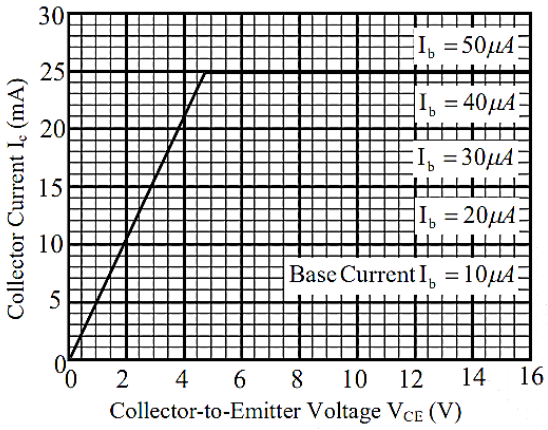
(c) 3.6μA

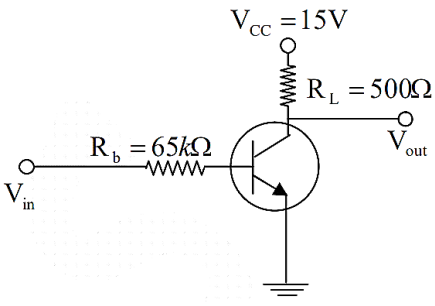
(d) 5.0μA

❖ TIFR PYQ

1. A plot of the common-emitter characteristics of a silicon n-p-n transistor is shown below. Given this information, and assuming that there will be a 0.7 V drop across a forward biased silicon p-n junction, the approximate value of the output voltage V_{out} for an input voltage $V_{\text{in}} =$ 2 V in the adjacent circuit will be

[TIFR 2009]





(a) 4 V

(b) 6 V

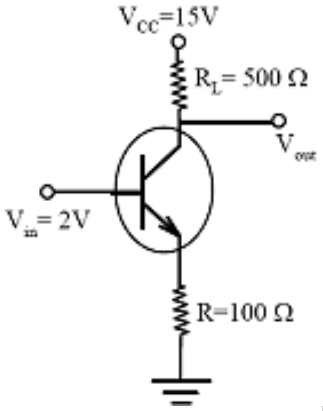
(c) 8 V

(d) 10 V

(e) 12 V

(f) 14 V

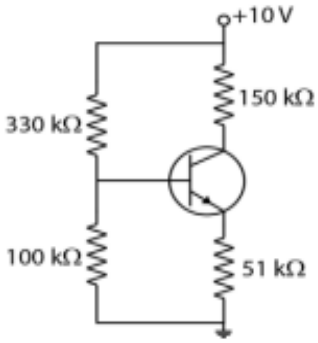
2. The circuit depicted on the right has been made with a silicon n-p-n transistor.
Assuming that there will be a 0.7 V drop across a forward-biased silicon p-n junction, the power dissipated across the transistor will be, approximately, **[TIFR 2013]**



(a) 53 mW (b) 94 mW

(c) 17 mW (d) 67 Mw

3. All resistors in the circuit on the right have a tolerance of $\pm 5\%$.
Assuming a diode drop of 0.7 V, which of the following is the lowest possible value of the collector voltage? **[TIFR 2014]**

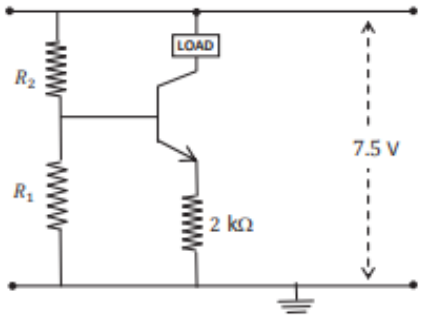


(a) 3.1 V (b) 4.1 V

(c) 4.7 V (d) 5.2 V

4. In the transistor circuit shown on the right, assume that the voltage drop between the base and the emitter is 0.5 V.
What will be the ratio of the resistances R_2/R_1, in order to make this circuit function as a source of constant current, $l = 1mA$?

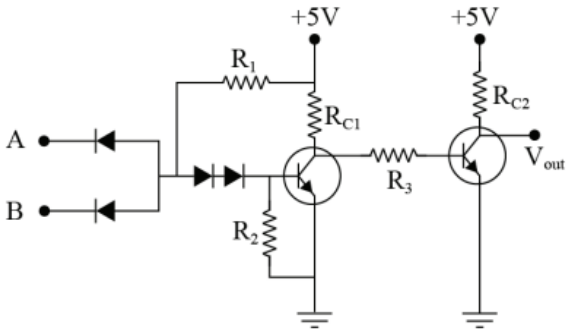
[TIFR 2016]



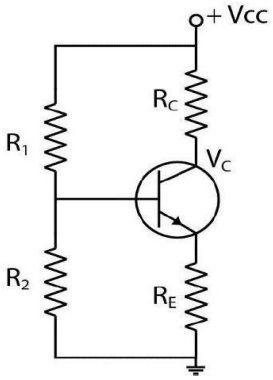
(a) 4.5 (b) 3.0

(c) 2.5 (d) 2.0

5. Which digital logic gate is mimicked by the following silicon diode and silicon transistor circuit? **[TIFR 2017]**



6. The circuit shown below represents a typical voltage-divider bias circuit for a transistor. Assume that resistance values and voltage values are typical for using the transistor as an amplifier. **[TIFR 2020]**



Which of the following changes in the circuit would result in an increase in the collector voltage V_C ?
(a) R_2 is decreased slightly

(b) R_2 is increased slightly

(c) R_c is decreased slightly

(d) R_c is increased slightly

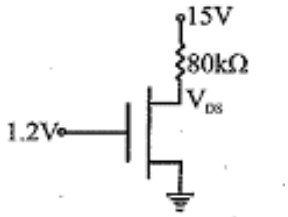
❖ Answer Key				
CSIR-NET				
1. a	2. c	3. a	4. b	5. d
6. d	7. d	8. a	9. b	10. c
11. d				
GATE				
1. c	2. c	3. d	4. a	5.
6. a	7. a	8. c	9. a	10.
11. 5.6to5.9	12. 5.7	13. 5	14. acd	15.
16. 12	17. 18.6μA			
JEST				
1. a	2. a	3. 1325Kω	4. a	5. b
6. 0950	7. c			
TIFR				
1.	2. b	3. b	4. d	5.
6. a				

GATE Q.15 : 2.20 to 2.36

TIFR Q. 5 : AND or (A.B)

❖ CSIR-NET PYQ

1. Consider an n-MOSFET with the following parameters: current drive strength $K = 60\mu\text{A/V}^2$, breakdown voltage $BV_{DS} = 10$ V, ratio of effective gate width to the channel length $\frac{W}{L} = 5$ and threshold voltage $V_{\text{th}} = 0.5$ V. In the circuit given below, this n-MOSFET is operating in the **[CSIR-DEC 2015]**



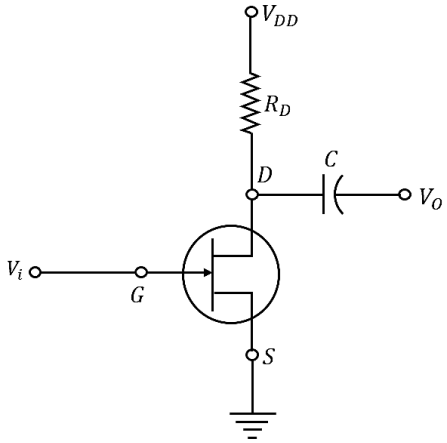
(a) ohmic region

(b) cut-off region

(c) saturation region

(d) breakdown region

2. In the n-channel JFET shown in figure below, $V_i = -2$ V, $C = 10$pF, $V_{DD} = +16$ V and $R_D = 2\text{k}\Omega$.

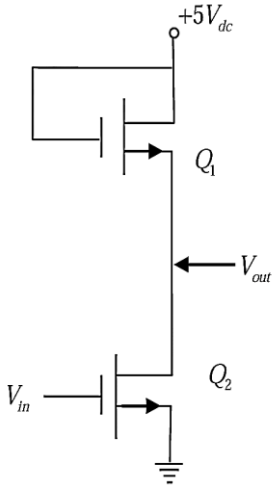


If the drain D-source S saturation current I_{Dss} is 10 mA and the pinch-off voltage V_P is -8 V, then the voltage across points D and S is **[CSIR-JUNE 2017]**

(a) 11.125 V (b) 10.375 V

(c) 5.75 V (d) 4.75 V

3. The circuit containing two n-channel MOSFETs shown below, works as **[CSIR-JUNE 2022]**



(a)a buffer

(b)an inverter

(c)a non-inverting amplifier

(d)a rectifier

❖ GATE PYQ

1. An n-channel silicon (dielectric constant = 12) FET with a channel width $a = 2 \times 10^{-6}$ m is doped with 10^{21} electrons /m^3. The pinch-off voltage is **[GATE 2001]**

(a) 0.86 V (b) 0.68 V

(c) 8.6 V (d) 6.8 V

2. The pinch-down voltage of a p-channel junction FET is $V_P = 5$ V and the drain-to-source saturation current $I_{DSS} = -40$ mA. The value of drain-source voltage V_{DS} is such that the transistor is operating in the saturated region. The drain current is given as $I_D = -15$ mA. Find the gate-source voltage V_{GS}. **[GATE 2001]**

3. A field effect transistor is a **[GATE 2004]**

(a)unipolar device

(b) special type of biopolar junction transistor

(c) unijunction device

(d) device with low input impedance

4. A junction field effect transistor behaves as a

[GATE 2005]

(a) voltage controlled current source

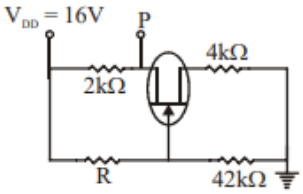
(b) voltage controlled voltage source

(c) current controlled voltage source

(d) current controlled current source

5. In the circuit shown, the voltage at test point P is 12 V and the voltage between gate and source is -2 V. The value of R (in $k\Omega$) is

[GATE 2007]



(a) 42 (b) 48

(c) 56 (d) 70

6. Under normal operating conditions, the gate terminal of an n-channel junction field effect transition (JFET) and an n-channel metal oxide semiconductor field effect transistor (MOSFET) are

[GATE 2008]

(a) both biased with positive potentials

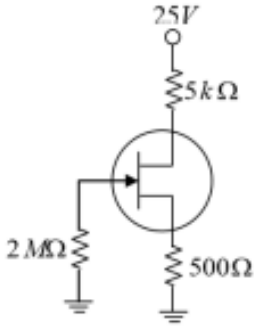
(b) both biased with negative potentials

(c) biased with positive and negative potentials respectively

(d) biased with negative and positive potentials respectively

7. In the given circuit, the voltage across the source resistor is 1V. The drain voltage (in V) is- _____.

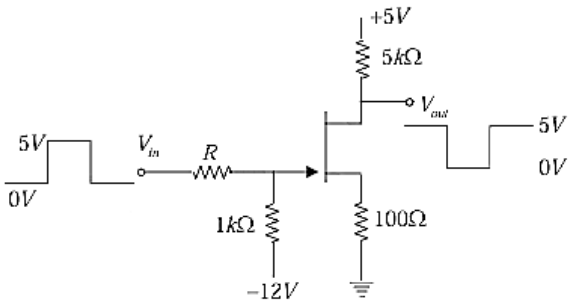
[GATE 2015]



8. An n - channel FET having Gate-Source switch-off voltage $V_{GS(OFF)} = -2V$ is used to invert a $0 - 5$ V square-wave signal as shown. The maximum allowed value of R would be

[GATE 2018]

(up to two decimal places).



❖ Answer Key				
CSIR-NET				
1. d	2. d	3. b		
GATE				
1. a	2. a	3. a	4. a	5. d
6. b	7. 15	8.		

Ans: GATE Q.8: 0.70 $k\Omega$

❖ **CSIR-NET PYQ**

1. Light of wavelength 660 nm and power of 1 mW is incident on a semiconductor photodiode with an absorbing layer of thickness of $(\ln\ 4)\mu$m.

(A) If the absorption coefficient at this wavelength is 10^4 cm^{-1} and if 1% power is lost on reflection at the surface, the power absorbed will be **[CSIR JUNE 2011]**

(a) 750μW (b) 675μW

(c) 250μW (d) 225μW

(B)The generated photo-current for a quantum efficiency of unity will be

(a) 360μA (b) 400μA

(c) 133μA (d) 120μA

2. A junction is made between a metal of work function W_M, and a doped semiconductor of work function W_S with $W_M > W_S$. If the electric field at the interface has to be increased by a factor of 3, then the dopant concentration in the semiconductor would have to be **[CSIR-DEC 2014]**

(a) increased by a factor of 9

(b) decreased by a factor of 3

(c) increased by a factor of 3

(d) decreased by a factor of $\sqrt{3}$

3. If the reverse bias voltage of a silicon varactor is increased by a factor of 2 , the corresponding transition capacitance **[CSIR-DEC 2015]**

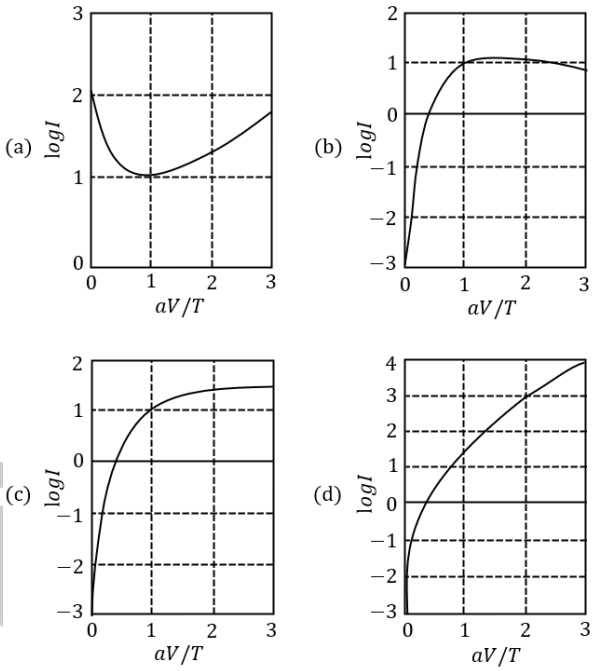
(a) increases by a factor of $\sqrt{2}$

(b) increases by a factor of 2

(c) decreases by a factor of $\sqrt{2}$

(d) decreases by a factor of 2

4. The $I-V$ characteristics of a device is $I = I_s\left[\exp\left(\frac{aV}{T}\right)-1\right]$, where T is the temperature and a and I_s are constants independent of T and V. Which one of the following plots is correct for a fixed applied voltage V ? **[CSIR-DEC 2016]**



5. Optical excitation of intrinsic germanium creates an average density of 10^{12} conduction electrons per cm^3 in the material at liquid nitrogen temperature. At this temperature, the electron and hole mobilities are equal, $\mu = 0.5 \times 10^4$ m^2 V^{-1} s^{-1}. The germanium dielectric constant is 20 . If 100 Volts is applied across 1 cm cube of crystal under these condition, about how much current, in mA, is observed? [Charge of electron $= 1.6 \times 10^{-19}$C] **[JEST 2022]**

6. A silicon crystal sample has 50 billion silicon atoms and 5 million free electrons. The silicon crystal is additionally doped with 5 million pentavalent atoms. Assume that the ambient thermal energy is much smaller than the bandgap of silicon. How many free electrons and holes are there inside the silicon crystal? **[JEST 2023]**

(a) Number of electrons is 30 million and number of holes is zero.

(b) Number of electrons is 10 million and number of holes is zero.

(c) Number of electrons is 10 million and number of holes is 5 million.

(d) Number of electrons is 5 million and number of holes is 5 million.

❖ GATE PYQ

1. A piece of semiconducting material is introduced into a circuit. If the temperature of the material is raised, the circuit current will **[GATE 2001]**

(a) increase (b) remain the same

(c) decrease (d) cease to flow

2. Which one of the following is TRUE for a semiconductor p junction with no external bias? **[GATE 2003]**

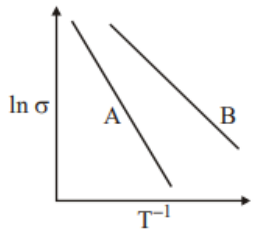
(a) The total charge in the junction is not conserved

(b) The p side of the junction is positively charged

(c) The p side of the junction is negative charged

(d) No charge develops anywhere in the junction

3. The temperature dependence of the electrical conductivity σ of two intrinsic semiconductors A and B is shown in the figure. If E_A and E_B are the band gaps of A and B respectively, which one of the following is TRUE? **[GATE 2004]**



(a) $E_A > E_B$

(b) $E_A < E_B$

(c) $E_A = E_B$

(d) E_A and E_B both depend on temperature

4. An intrinsic semiconductor with mass of a hole m_h and mass of an electron m_e is at a finite temperature T. If the top of the valence band energy is E_v and the bottom of the conduction band energy is E_c, the Fermi energy of the semiconductor is **[GATE 2008]**

(a) $E_F = \left(\frac{E_y + E_c}{2}\right) - \frac{3}{4}k_B T \ln\left(\frac{m_h}{m_c}\right)$

(b) $E_F = \left(\frac{k_B T}{2}\right) + \frac{3}{4}(E_v + E_c)\ln\left(\frac{m_h}{m_c}\right)$

(c) $E_F = \left(\frac{E_v + E_c}{2}\right) + \frac{3}{4}k_B T \ln\left(\frac{m_h}{m_c}\right)$

(d) $E_F = \left(\frac{k_B T}{2}\right) - \frac{3}{4}(E_v + E_c)\ln\left(\frac{m_h}{m_c}\right)$

5. A phosphorous doped silicon semiconductor (doping density: $10^{17}/\text{cm}^3$) is heated from 100°C to 200°C. which one of the following statements is correct? **[GATE 2013]**

(a) position of fermi level moves towards conduction band

(b) position of dopant level moves towards conduction band

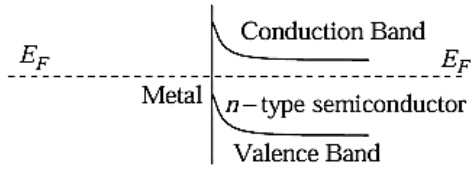
(c) position of fermi level moves towards middle of energy gap

(d) position of dopant level moves towards middle of energy gap

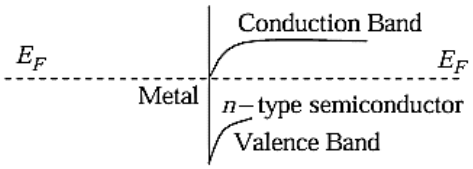
6. The number density of electron in the conduction band of a semiconductor at a given temperature is $2 \times 10^{19}\ \text{m}^{-3}$. Upon lightly doping this semiconductor with donor impurities, the number density of conduction electrons at the same temperature becomes $4 \times 10^{20}\ \text{m}^{-3}$. The ratio of majority to minority charge carrier concentration is_____. **[GATE 2016]**

7. A junction is formed between a metal on the left and an n-type semiconductor on the right. Before forming the junction, the Fermi level E_F of the metal lies below that of the semiconductor. Then which of the following schematics are correct for the bands and the $I-V$ characteristics of the junction? **[GATE 2022]**

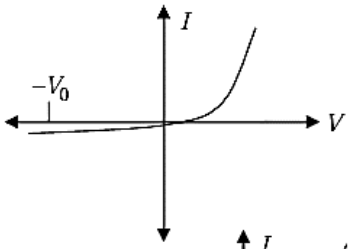
(a)



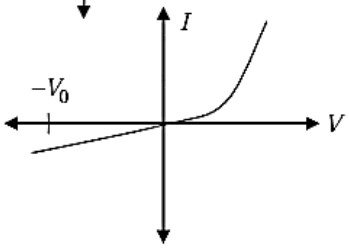
(b)



(c)



(d)



❖ TIFR PYQ

1. The sign of the majority charge carriers in a doped silicon crystal is to be determined experimentally. In addition to a voltage supply, the combination of instruments needed to perform the experiment is **[TIFR 2011]**

(a) Thermometer, Voltmeter and Ammeter

(b) Pickup Coil, Voltmeter and Ammeter

(c) Magnet, Voltmeter and Ammeter

(d) Heater, Magnet and Thermometer

❖ Answer Key				
CSIR-NET				
1. c/c	2. a	3. c	4. d	5. 0.333
6. b				
GATE				
1. a	2. c	3. a	4. c	5. c
6. 400	7. ac/ad			
TIFR				
1.				

Transient Circuit

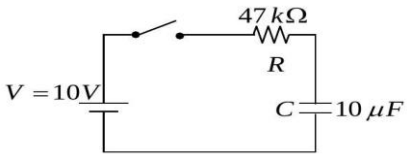
❖ CSIR-NET PYQ

1. An inductor L, a capacitor C and a resistor R are connected in series to an AC source, $V = V_0 \sin\ \omega t$. If the net current is found to depend only on R, then **[CSIR-JUNE 2020]**

(a) $C = 0$ (b) $L = 0$

(c) $\omega = 1/\sqrt{LC}$ (d) $\omega = \sqrt{\frac{1}{LC} - \frac{R^2}{4L^2}}$

2. A 10 V battery is connected in series to a resistor R and a capacitor C, as shown the figure.

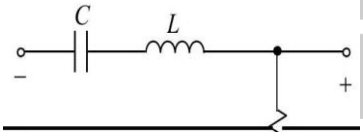


The initial charge on the capacitor is zero. The switch is turned on and the capacitor is allowed to charge to its full capacity. The total work done by the battery in this process is **[CSIR-JUNE 2020]**

(a) 10^{-3} J (b) 2×10^{-3} J

(c) 5×10^{-4} J (d) $47 \times 10^{-2} J$

3. In the LCR circuit shown below, the resistance $R = 0.05\Omega$, the inductance $L = 1H$ and the capacitance $C = 0.04$ F.



If the input v_{in} is a square wave of angular frequency 1rad/s the output v_{out} is best approximated by a **[CSIR-JUNE 2021]**

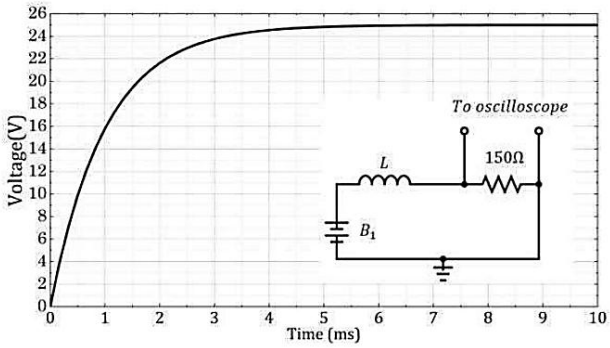
(a) square wave of angular frequency 1rad/s

(b) sine wave of angular frequency 1rad/s

(c) square wave of angular frequency 5rad/s

(d) sine wave of angular frequency 5rad/s

4. An ideal inductor L is connected in series to a 150Ω resistor as shown in the circuit (inset). When the circuit is driven by a battery B_1, the voltage across the resistor as a function of time, as measured by an oscilloscope, is shown in the plot.



Based on this observation, the estimated value of L is closest to **[CSIR DEC 2024]**

(a)50 mH (b)300 mH

(c)450 mH (d)150 mH

❖ GATE PYQ

1. For high frequencies ($\omega \to \infty$) the input impedance is **[GATE 2003]**

(a) 0 (b) R

(c) $R/(1 + \omega RC)$ (d) ∞

2. For low frequencies ($\omega \to \infty$) the input impedance is **[GATE 2003]**

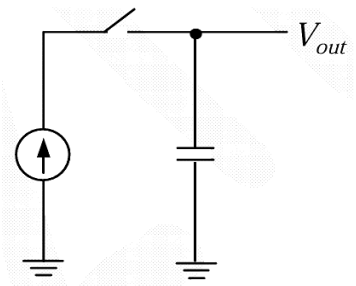
(a) $V_0 = (1/RC)\int V_1 dt$

(b) The voltages at the inverting and non-inverting terminals of the op-amp are nearly

(c) The voltage at the non-inverting terminal of the op-amp and the current in the resistor attached to it are $\pi/2$ out of phase

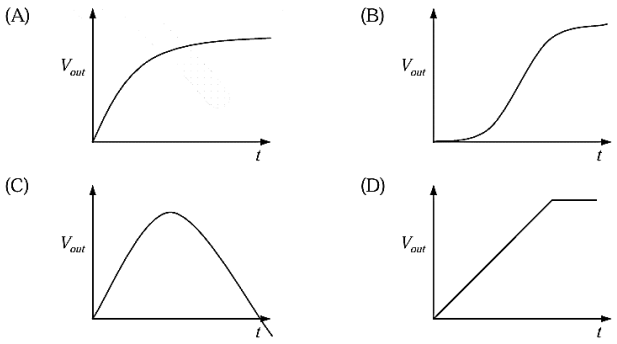
(d) The current in the two resistors are in phase

3. The figure shows a constant current source charging a capacitor that is initially unchanged **[GATE 2010]**



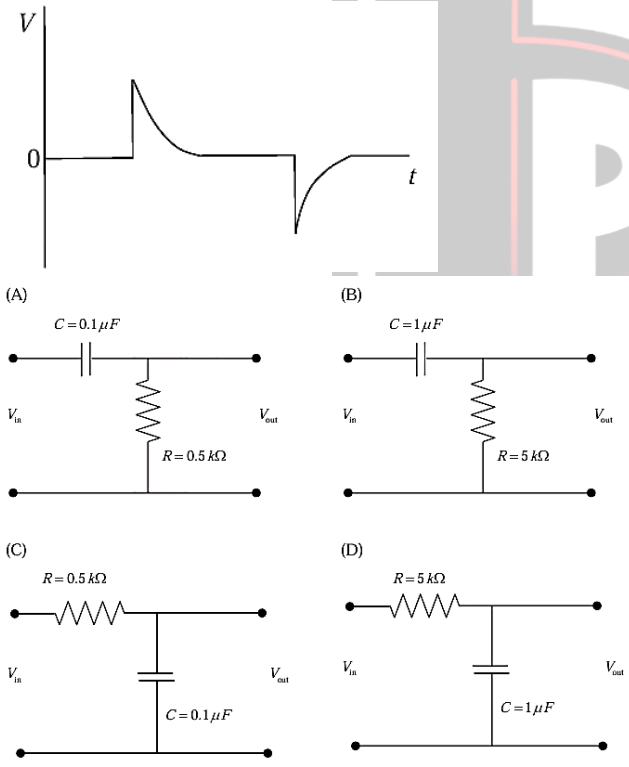
If the switch is closed at $t = 0$, which of the following plots depicts correctly the output voltage of the circuit as a function of time?

[GATE 2010]



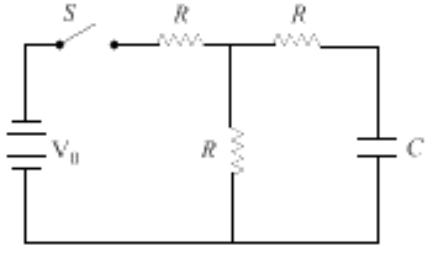
4. An input voltage in the form of a square wave of frequency 1kHz is given to a circuit, which results in the output shown schematically below. Which one of the following options is the CORRECT representation of the circuit?

[GATE 2023]



❖ JEST PYQ

1. A capacitor C is connected to a battery V_0 through three equal resistors R and a switch S as shown below:



The capacitor is initially uncharged. At time $t = 0$, the switch S is closed. The voltage across the capacitor as a function of time ' t ' for $t > 0$ is given by **[JEST 2012]**

(a) $(V_0/2)(1 - \exp(-t/2Rc))$

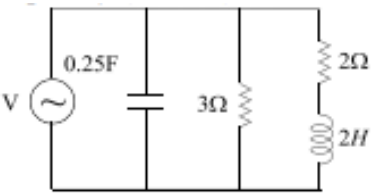
(b) $(V_0/3)(1 - \exp(-t/3Rc))$

(c) $(V_0/3)(1 - \exp(-3t/2Rc))$

(d) $(V_0/2)(1 - \exp(-2t/3Rc))$

2. Find the resonance frequency (rad/sec) of the circle shown in the figure below

[JEST 2013& JEST 2014]

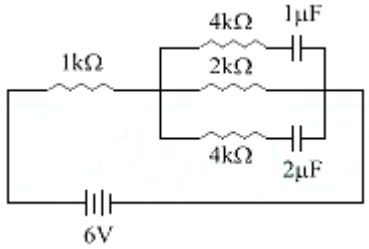


(a) 1.41 (b) 1.0

(c) 2.0 (d) 1.73

3. Consider the following circuit in steady state condition. Calculate the amount of charge stored in $1\mu F$ and $2\mu F$ capacitors respectively.

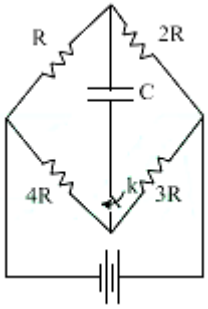
[JEST 2017]



(a) $4\mu C$ and $8\mu C$ (b) $8\mu C$ and $4\mu C$

(c) $3\mu C$ and $6\mu C$ (d) $6\mu C$ and $3\mu C$

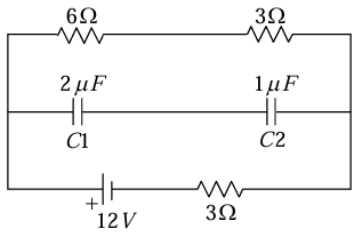
4. In the circuit shown below, the capacitor is initially uncharged. Immediately after the



Key K is closed, the reading in the ammeter is

27 mA. What will the reading (in mA) be a long time later ? **[JEST 2018]**

5. What is the charge stored on each capacitor C_1 and C_2 in the circuit shown in the given figure? **[JEST 2020]**



(a) $6\mu C, 6\mu C$ (b) $6\mu C, 3\mu C$

(c) $3\mu C, 6\mu C$ (d) $3\mu C, 3\mu C$

6. A capacitor with capacitance C is connected in series with a resistor of resistance R and an ideal DC source with voltage V_S. At one instant during the charging of the capacitor if the resistor is replaced by a wire of zero resistance, which of the following statements is true?

(a)The voltage across the capacitor will increase slowly.

(b)None of the others is true.

(c)The capacitor immediately attains the source voltage V_S.

(d)The voltage across the capacitor will drop immediately to zero.

❖ TIFR PYQ

1. Two parallel plates of metal sandwich a dielectric pad of thickness d, forming an ideal capacitor of capacitance C. The dielectric pad is elastic, having a spring constant k. If an ideal battery of voltage V across its terminals is connected to the two plates of this capacitor, the fractional change $\delta d/d \ll 1$ in the gap between the plates is **[TIFR 2009]**

(a) zero (b) $+\dfrac{\frac{1}{2}CV^2}{kd^2}$

(c) $-\dfrac{\frac{1}{2}CV^2}{kd^2+CV^2}$ (d) $-\dfrac{\frac{1}{2}CV^2}{kd^2-CV^2}$

2. Two LCR circuits (A) and (B) are shown below where $C_c \ll C$. At time $t = 0$, a charge Q is put on the capacitor C.

Which of the following statements is correct? **[TIFR 2014]**

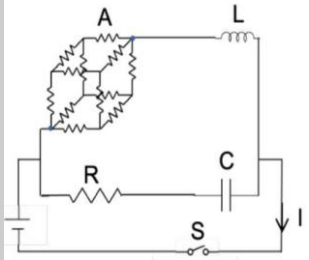
(a) The charge Q will decay faster in (A)

(b) The charge Q will decay faster in (B)

(c) The charge Q will decay at the same rate in (A) and (B)

(d) The relative decay rates cannot be predicted without knowing the exact values of L, C, R and C_c

3. The circuit diagram on the right shows a block A representing a cubic structure comprising 12 identical resistances of 120Ω each, whose body diagonal vertices are connected to the rest of the circuit with an inductor L = 10mH, a resistor R = 100Ω, and a capacitor C = 1μF. Now, the switch S is turned on at $t = 0$. The



earliest time at which the current reaches a steady value I_0 is **[TIFR 2022]**

(a) infinite (b) $100\mu s$

(c) $200\mu s$ (d) zero

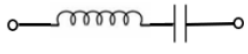
4. It is required to design a circuit with an impedance $Z(\omega)$ such that

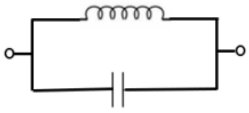
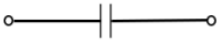
$$Z(\omega) = ik(\omega - \omega_0)$$

for a range of frequencies ω such that

$$|\omega - \omega_0|/\omega_0 \ll 1$$

where k and ω_0 are constant real numbers. A possible design for this circuit would correspond to **[TIFR 2022]**

(a)  (b) 

(c)  (d) 

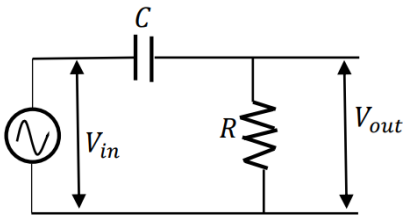
5. The sinusoidal signal

$$V_{in} = V_i \sin(2\pi f t)$$

is given to a high-pass filter (see Figure). The output signal is given by

$$V_{\text{out}} = V_i |A| \sin(2\pi f t + \phi).$$

What is the value of $|A|$? **[TIFR 2025]**



(a) $\dfrac{1}{\left|1+\left(\dfrac{1}{2\pi RCf}\right)^2\right|^{1/2}}$ (b) $\dfrac{1}{\left|1+\left(\dfrac{1}{2\pi RCf}\right)\right|}$

(c) $\dfrac{1}{\left|1+\left(\dfrac{1}{2\pi RCf}\right)^2\right|}$ (d) $\dfrac{1}{\left|1+\left(\dfrac{1}{2\pi RCf}\right)\right|^{1/2}}$

❖ Answer Key				
CSIR-NET				
1. c	2. a	3. d	4. d	
GATE				
1. b	2. a	3. d	4. a	
JEST				
1. d	2. b	3. a	4. 0030	5. a
6. **c**				
TIFR				
1.	2. a	3. d	4. a	5. a

ADC & DAC

❖ CSIR-NET PYQ

1. A signal of frequency 10kHz is being digitized by an A/D converter. A possible sampling time which can be used is: **[CSIR-JUNE 2011]**

(a) $100\mu s$ (b) $40\mu s$

(c) $60\mu s$ (d) $200\mu s$

2. If the analog input to an 8-bit successive approximation ADC is increased from 1.0 V to 2.0 V, then the conversion time will **[CSIR-JUNE 2013]**

(a) remain unchanged

(b) double

(c) decrease to half its original value

(d) increase four times

3. The full scale voltage of an n-bit Digital-to-Analog Converter is V. The resolution that can be achieved in it is **[CSIR-DEC 2017]**

(a) $\frac{V}{(2^n-1)}$ (b) $\frac{V}{(2^n+1)}$

(c) $\frac{V}{2^{2n}}$ (d) $\frac{V}{n}$

4. The full scale of a 3-bit digital-to-analog (DAC) converter is 7 V. Which of the following tables represents the output voltage of this 3-bit DAC for the given set of input bits? **[CSIR-JUNE 2018]**

(a)

Input bits	Output voltage
000	0
001	1
010	2
011	3

(b)

Input bits	Output voltage
000	0
001	1.25
010	2.5
011	3.75

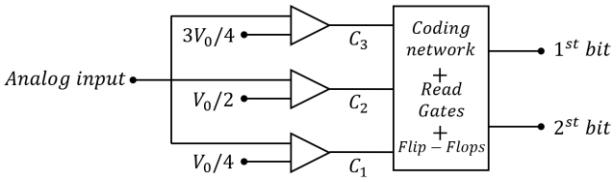
(c)

Input bits	Output voltage
000	1.25
001	2.5
010	3.75
011	5

(d)

Input bits	Output voltage
000	1
001	2
010	3
011	4

5. The figure below shows a 2-bit simultaneous analog-to-digital (A/D) converter operating in the voltage range 0 to V_0. The output of the comparators are C_1, C_2 and C_3 with the reference inputs $\frac{V_0}{4}, \frac{V_0}{2}$ and $\frac{3V_0}{4}$, respectively.



The logic expression for the output corresponding to the less significance bit is **[CSIR-DEC 2019]**

(a) $C_1C_2C_3$ (b) $C_2\bar{C_3}+\bar{C_1}$

(c) $C_1\bar{C_2}+C_3$ (d) $C_2\bar{C_3}+C_2$

❖ GATE PYQ

1. The reference voltage of an analog to digital The largest analog output voltage from a 6-bit digital to analog converter (DAC) which produces 1.0 V output for a digital input of 010100, is **[GATE 2006]**

(a) 1.6 V (b) 2.9 V

(c) 3.15 V (d) 5.0 V

2. An analog voltage V is converted into 2-bit binary number. The minimum number of comparators required and their reference voltage are **[GATE 2008]**

(a) $3, \left(\frac{V}{4}, \frac{V}{2}, \frac{3V}{4}\right)$ (b) $3, \left(\frac{V}{3}, \frac{2V}{3}, V\right)$

(c) $4, \left(\frac{V}{5}, \frac{2V}{5}, \frac{3V}{5}, \frac{4V}{5}\right)$ (d) $4, \left(\frac{V}{4}, \frac{V}{2}, \frac{3V}{4}, V\right)$

3. What should be the clock frequency of a 6-bit A/D converter so that its maximum conversion time is $32\mu s$? **[GATE 2013]**

(a) 1MHz (b) 2MHz

(c) 0.5MHz (d) 4MHz

4. A 3-bit analog-to-digital converter is designed to digitize analog signals ranging from 0 V to 10 V. For this converter, the binary output corresponding to an input of 6 V is **[GATE 2019]**

(a) 011 (b) 101

(c) 100 (d) 010

❖ **JEST PYQ**

1. converter is 1 V. The smallest voltage step that the converter can record using a 12 -bit converter is, **[JEST 2015]**

(a) 0.24 V (b) 0.24Mv

(c) $0.24\mu V$ (d) 0.24Nv

2. A 16-bit analog to digital converter works in the range $0 - 1$ Volt. The least count of the converter is **[JEST 2020]**

(a) 0.30mV (b) 15.26mV

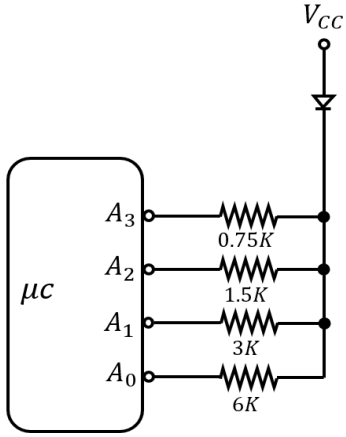
(c) $5.44nV$ (d) $15.26\mu V$

3. A 12-bit analog-to-digital converter has an operating range of 0 to 1 V. The smallest voltage step (in mV, upto two significant digits) that one can record using this converter is **[JEST 2022]**

❖ Answer Key				
CSIR-NET				
1. c	2. a	3. a	4. a	5. c
GATE				
1. c	2. a	3. a	4. c	
JEST				
1. b	2. d	3. 0.24		

❖ CSIR-NET PYQ

1. The pins 0,1,2, and 3 of part A of a microcontroller are connected with resistors to drive an LED at various intensities as shown in the figure.



For $V_{co} = 4.2$ V and a voltage drop of 1.2 V across the LED, the range (maximum current) and resolution (Step size) of the drive current are, respectively, **[CSIR-DEC 2011]**

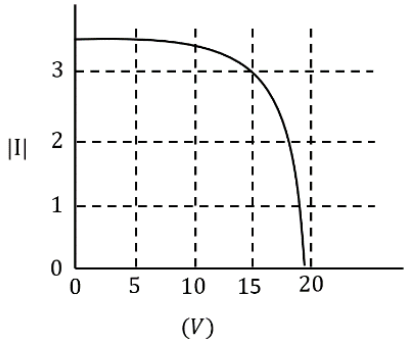
(a) 4.0 mA and 1.0 mA

(b) 15.0 mA and 1.0 mA

(c) 7.5 mA and 0.5 mA

(d) 4.0 mA and 0.5 mA

2. The output characteristics of a solar panel at a certain level of irradiance is shown in the figure below.



If the solar cell is to power a load of 5Ω, the power drawn by the load is: **[CSIR-DEC 2012]**

(a) 97 W (b) 73 W

(c) 50 W (d) 45 W

3. The input to a lock-in amplifier has the form $V_i(t) = V_i \sin(\omega t + \theta_i)$ where V_i, ω, θ_i are the amplitude, frequency and phase of the input signal respectively. This signal is multiplied by a reference signal of the same frequency ω, amplitude V_r and phase θ_f. If the multiplied signal is fed to a low pass filter of cut-off frequency ω, then the final output signal is **[CSIR-JUNE 2013]**

(a) $\frac{1}{2} V_i V_r \cos(\theta_i - \theta_r)$

(b) $V_i V_r \left[\cos(0_i - 0_r) - \cos\left(\frac{1}{2}\omega t + \theta_i + \theta_r\right)\right]$

(c) $V_i V_r \sin(\theta_i - \theta_r)$

(d) $V_i V_r \left[\cos(\theta_i - \theta_r) + \cos\left(\frac{1}{2}\omega t + \theta_i + \theta_r\right)\right]$

4. If the reverse bias voltage of a silicon varactor is increased by a factor of 2, the corresponding transition capacitance **[CSIR-DEC 2015]**

(a) increases by a factor of $\sqrt{2}$

(b) increases by a factor of 2

(c) decreases by a factor of $\sqrt{2}$

(d) decreases by a factor of 2

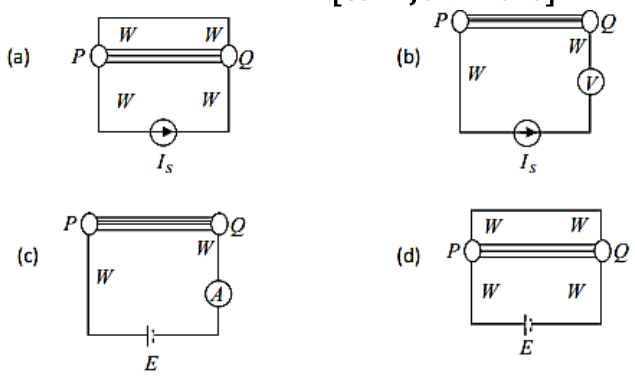
5. A receiver operating at 27°c has an input resistance of 100Ω. The input thermal noise voltage for this receiver with a bandwidth of 100kHz is closest to **[CSIR-JUNE 2022]**

(a)0.4nV (b)0.6pV

(c)40mV (d)0.4μV

6. A circuit needs to be designed to measure the resistance R of a cylinder PQ to the best possible accuracy, using an ammeter A, a voltmeter V, a battery E and a current source I_S (all assumed to be ideal). The value of R is known to be approximately 10Ω, and the resistance W of each of the connecting wires is close to 10Ω. If the current from the current source and voltage from the battery are known exactly, which of the following circuits provides the most accurate measurement of R ?

[CSIR-JUNE 2023]



(a) B (b) A

(c) C (d) D

7. A piezoresistive pressure sensor utilizes change in electrical resistance (ΔR) with change in pressure (ΔP) as $\Delta R = -R_0 \log_{10}\left(\frac{\Delta P}{P_0}\right)$, where $R_0 = 500\Omega$ and $P_0 = 1000$mbar. A current of 2μA is passed through the sensor and the resultant voltage drop is measured using an analog-to-digital (ADC) converter having a range 0 to 1 V . If a pressure change of 1 mbar is to be measured, amongst the given options, the minimum number of bits needed for the ADC is

[CSIR JUNE 2024]

(a)12 (b)14

(c)8 (d)10

❖ TIFR PYQ

1. Consider a very, very thin wire of uniformly circular cross section. The diameter of the wire is of the order of microns. The correct equipment required to measure the precise value of resistivity of this wire is

[TIFR 2009]

(a) ammeter, voltmeter, scale, slide calipers

(b) ammeter, magnet, screw gauge, thermometer

(c) voltmeter, magnet, screw gauge, scale

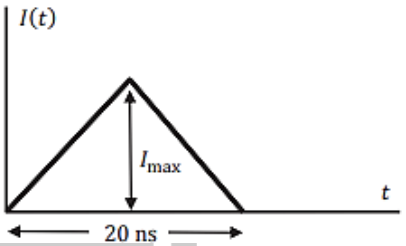
(d) ammeter, voltmeter, scale, monochromatic laser source

2. In a scanning tunnelling microscope, a fine Platinum needle is held close to a metallic surface in vacuum and electrons are allowed to tunnel across the tiny gap δ between the surface and the needle. The tunnelling current I is related to the gap δ, through positive constants a and b, as [TIFR 2012]

(a) $I = a - b\delta$ (b) $I = a + b\delta$

(c) $\log I = a - b\delta$ (d) $\log I = a + b\delta$

3. A photomultiplier tube is used to detect identical light pulses each of which consists of a fixed number of photons. The photoelectric efficiency is 10%, i.e. a photon has 10% probability of causing the emission of a detectable photoelectron. The photomultiplier gain is 10^6.



The typical output current, as a function of time, is shown by the figure below for a few pulses, where I_{max} is 80μA. It follows that the number of photons in each pulse is

(a) 5×10^6 (b) 5

(c) 800 (d) 50

4. On passing electric current, a tungsten filament is emitting electrons by thermionic emission. In order to maintain the energy of the electron beam obtained from this source at a value approximately 100eV, which of the following methods will work in practice? [TIFR 2020]

(a) Float the filament at -100 Volts with a grounded aperture in front of it.

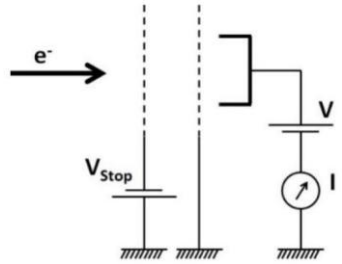
(b)Heat the filament so that the emitted electrons will have 100eV kinetic energy due to temperature.

(c)Apply a +100 Volts potential with respect to the filament potential to an aperture kept very close to the filament.

(d)Use an appropriate magnetic field to draw out the electron beam at the desired energy without applying any electric field.

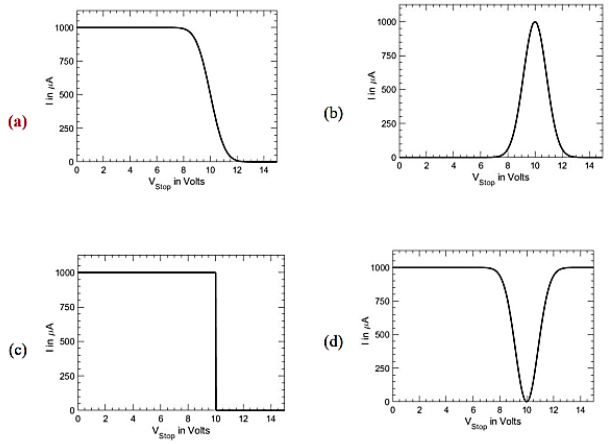
5. A well-collimated constant-current electron beam of Gaussian energy distribution centered

at 10eV with FWHM of 2eV is detected using a metal cup connected to an ammeter, as shown in the figure below. The entire apparatus is kept in vacuum.

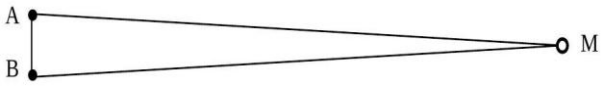


To measure the energy width of the electron beam, a grid is introduced with a voltage source V_{stop} connected to it, as shown in the figure. The current measured in the cup is plotted as a function of the value of V_{stop}. The graph of the current I vs V_{stop} would be

[TIFR 2023]

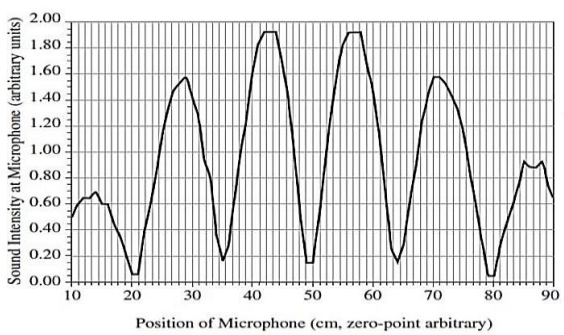


6. Two small loudspeakers A and B, separated by 15 cm, were pointed toward a small microphone M at a distance 1.5 m away from the centre of the line AB, in the perpendicular direction as shown in the sketch below.



The following sound intensity pattern was observed as a function of the position of the microphone as it is moved parallel to AB.

[TIFR 2024]



The dips in the signal were repeated at the interval of 14.5 cm. The speed of sound in the experiment's background condition is 343 m/s. What can we conclude from this information?

[TIFR 2024]

(a) The two loudspeakers are vibrating at frequency 23.65kHz and they are out of phase.

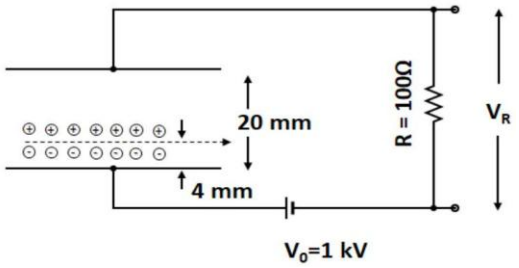
(b) The two loudspeakers are vibrating at frequency 23.65kHz and they are in phase.

(c) The two loudspeakers are vibrating at frequency 47.3kHz and they are in phase.

(d) The two loudspeakers are vibrating at frequency 47.3kHz and they are out of phase.

7. Consider a charge particle detection chamber as shown in the figure below. The chamber is made of a set of parallel plates separated by 20 mm distance and connected to the external resistance (R = 100Ω) as shown in the figure along with the high voltage power supply of 1kV.

[TIFR 2024]



The chamber is filled with Argon (Ar) gas (ionization energy 16eV). If a charged particle passes through the chamber and loses sufficient energy, it ionizes the Ar atoms and generates a small voltage pulse across the resistance R.

In an experiment, an alpha particle of energy 5.5MeV enters the chamber at a distance of 4 mm from the bottom plate, as shown, generating ion-electron pairs. If the effective capacitance of the chamber is 100pF, the measured voltage pulse shape would be best described as:

(a) No voltage pulse would be generated as both electrons and ions will neutralize the charge collected by the capacitor

(b) Two sharp voltage pulses of equal magnitude and opposite signs

(c) Two sharp voltage pulses of the same magnitude and sign

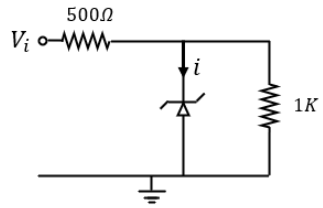
(d) A sharp voltage pulse followed by a very weak broad pulse

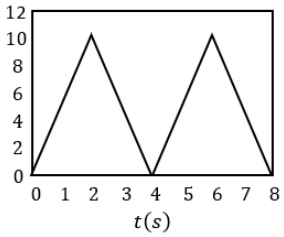
❖ Answer Key				
CSIR-NET				
1. c	2. d	3. a	4. c	5. d
6. b	7. d			
TIFR				
1.	2. c	3. a,b	4. a	5. a
6.	7. d			

Wave Shaping

❖ CSIR-NET PYQ

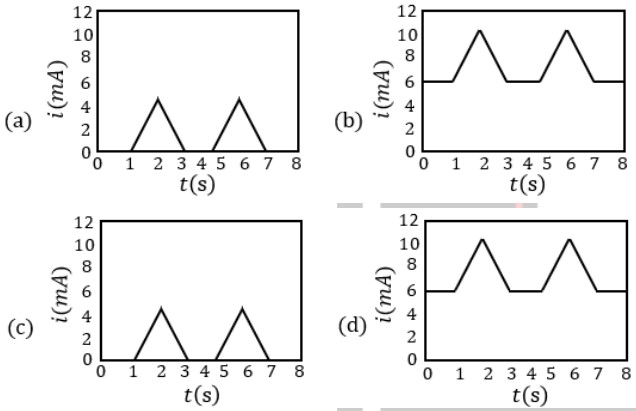
1. The figure below shows a voltage regulator utilizing a Zener diode of breakdown voltage 5 V and a positive triangular wave input of amplitude 10 V.





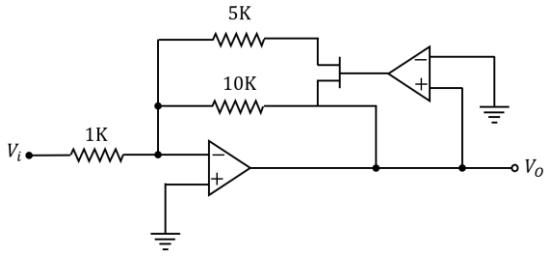
For $V_i > 5$ V, the Zener regulates the output voltage bychanneling the excess current through it self. Which of the following waveforms shows the current 'i' passing through the Zener diode?

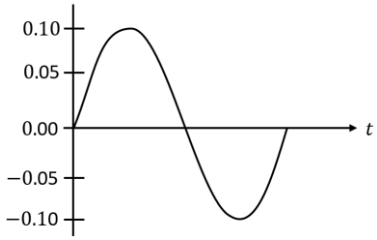
[CSIR-DEC 2011]



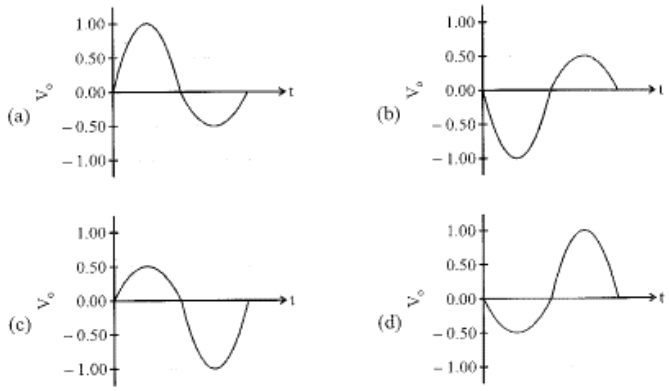
2. For the circuit and the input sinusoidal waveform shown in the figures below, which is the correct waveform at the output?

[CSIR-JUNE 2015]



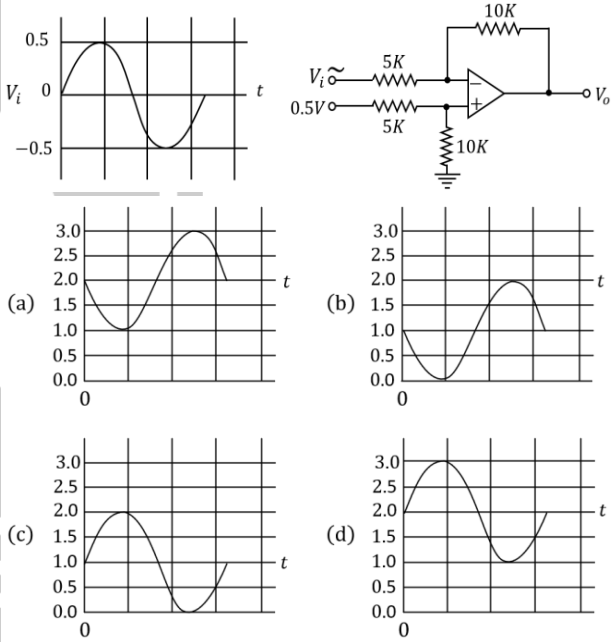


(The time scales in all the plots are the same).

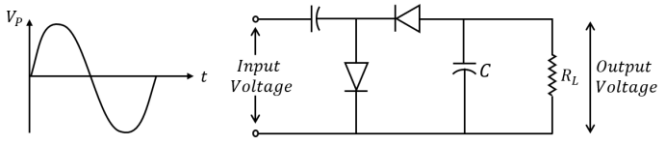


3. Given the input voltage V_i, which of the following waveforms correctly represents the output voltage V_0 in the circuit shown below?

[CSIR-JUNE 2016]



4. A sinusoidal signal with a peak voltage V_p and average value zero, is an input to the following circuit.



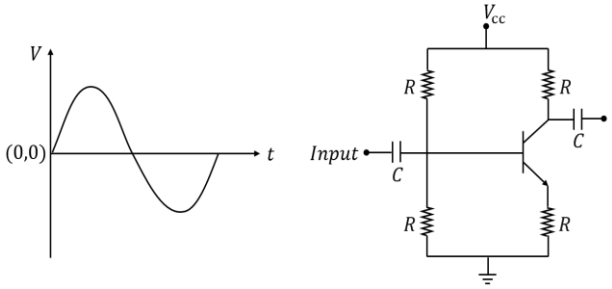
Assuming ideal diodes, the peak value of the output voltage across the load resistor R_L, is

[CSIR-JUNE 2018]

(a) V_P (b) $V_P/2$

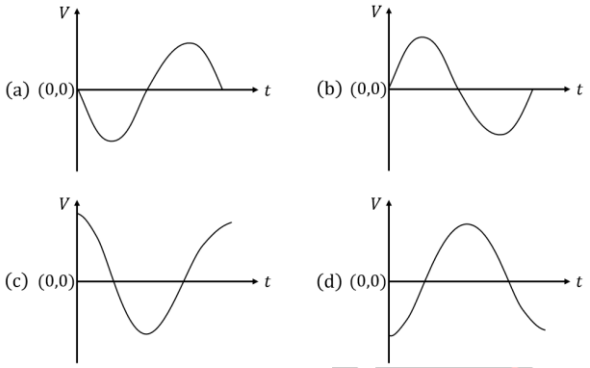
(c) $2V_P$ (d) $\sqrt{2}V_P$

5. A sinusoidal signal is an input to the following circuit:

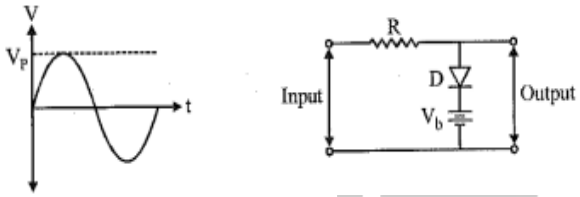


Which of the following graphs best describes the output waveform?

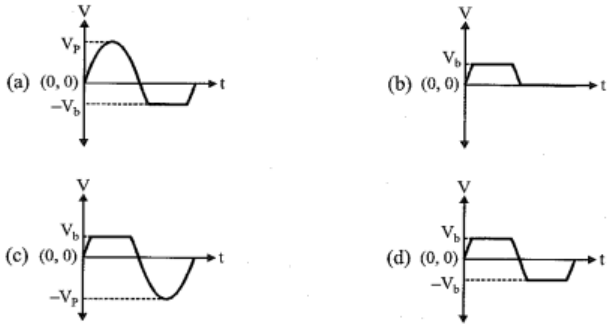
[CSIR-DEC 2018]



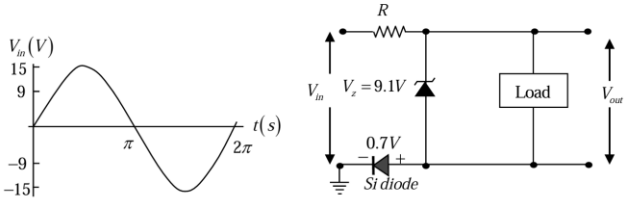
6. A sinusoidal voltage having a peak value of V_P is an input to the following circuit, in which the DC voltage is V_b. **[CSIR-DEC 2018]**



Assuming an ideal diode, which of the following best describes the output waveform?

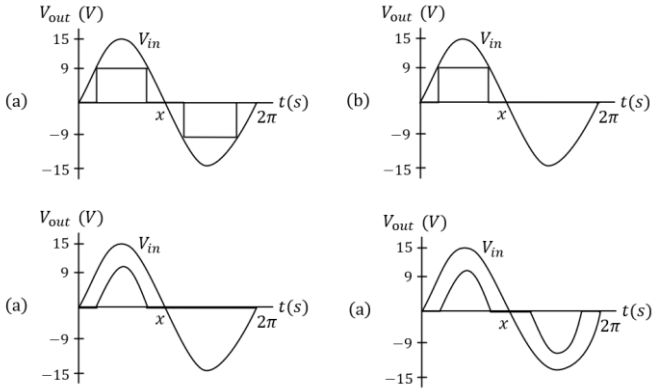


7. A high impedance load network is connected in the circuit as shown below



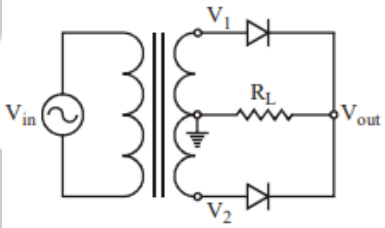
The forward voltage drop for silicon diode is 0.7 V and the Zener voltage is 9.10 V. If the input voltage (V_{in}) is sine wave with an amplitude of 15 V (as shown in the figure above), which of the following waveform qualitatively describes the output voltage (V_{out}) across the load?

[CSIR-JUNE 2022]



❖ GATE PYQ

1. For the rectifier circuit shown in the figure, the sinusoidal voltage (V_1 or V_2) at the output of the transformer has a maximum value of 10 V. The load resistance R_L is $k\Omega$. If I_{ave} is the average current through the resistor R_L the circuit corresponds **[GATE 2005]**



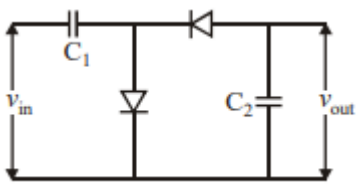
(a) full wave rectifier with $I_{av} = 20/\pi$mA

(b) half wave rectifier with $I_{av} = 20/\pi$mA

(c) half wave rectifier with $I_{av} = 10/\pi$mA

(d) full wave rectifier with $I_{av} = 10/\pi$mA

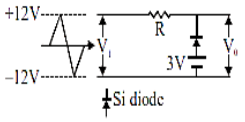
2. A sinusoidal input voltage v_{in} of frequency ω is fed to the circuit shown in the figure, where $C_1 \gg C_2$. If v_m is the peak value of the input voltage, then output voltage (v_{out}) is **[GATE 2006]**



(a) $2v_m$ (b) $2v_0 \sin \omega t$

(c) $\sqrt{2}v_m$ (d) $\frac{v_m}{2} \sin \omega t$

3. When an input voltage V_i, of the form shown, is applied to the circuit given below, the output voltage V_0 is of the form **[GATE 2007]**



4. If the peak output voltage of a full wave rectifier is 10 V, its d.c. voltage is **[GATE 2012]**

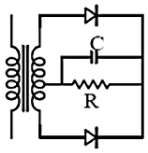
(a) 10.0 V (b) 7.07 V

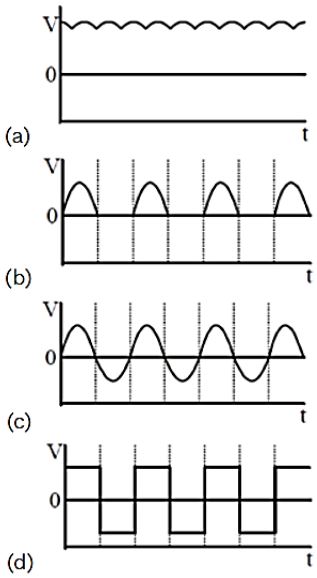
(c) 6.36 V (d) 3.18 V

5. A voltage regulator has ripple rejection of -50 dB. If input ripple is 1mV, what is the output ripple voltage in μV ? The answer should be up to two decimal places_____.

[GATE 2013]

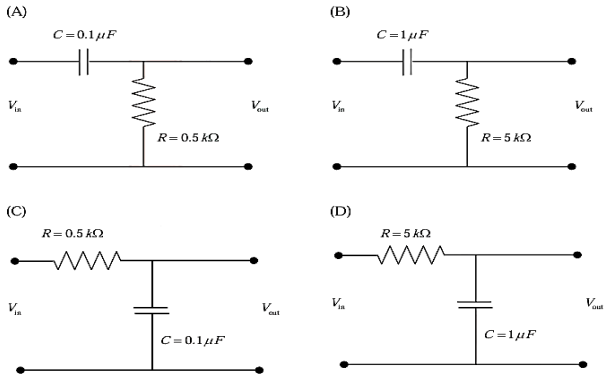
6. In the figure given below, the input to the primary of the transformer is a voltage varying sinusoidally with time. The resistor R is connected to the centre tap of the secondary. Which one of the following plots represents the voltage across the resistor R as a function of time? **[GATE 2017]**





7. An input voltage in the form of a square wave of frequency 1kHz is given to a circuit, which results in the output shown schematically below. Which one of the following options is the CORRECT representation of the circuit?

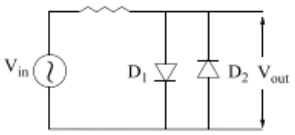
[GATE 2023]

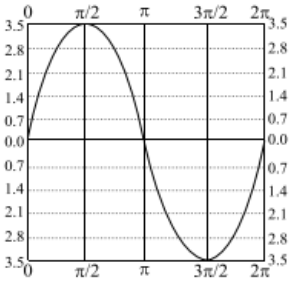


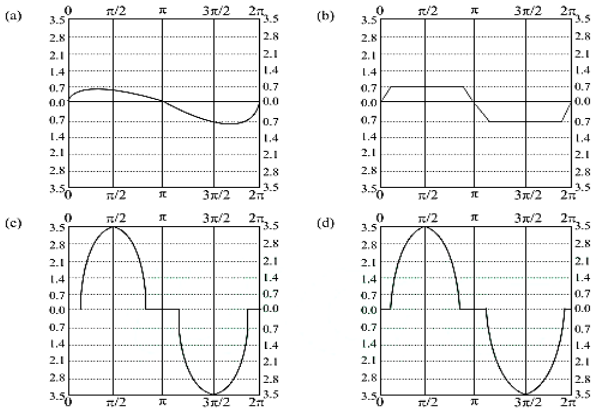
❖ JEST PYQ

1. In the following silicon diode circuit ($V_B = 0.7$ V), determine the output waveform (V_{out}) for the given input wave.

[JEST 2017]

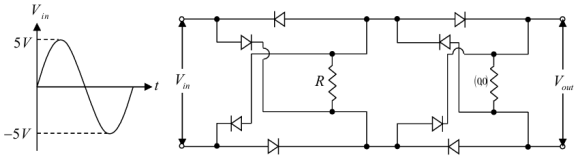




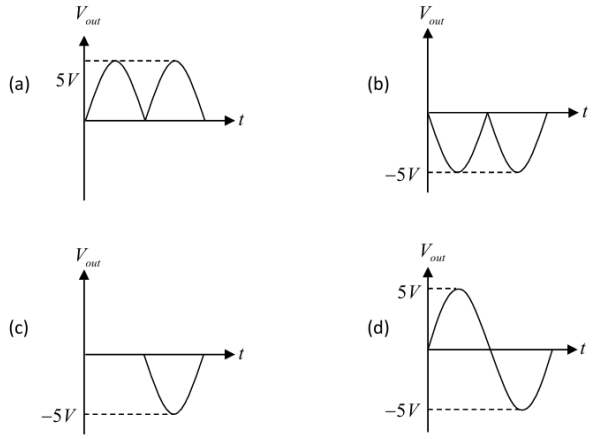


2. The circuit given in the figure below is composed of ideal diodes and resistances R. The input waveform is shown on the left.

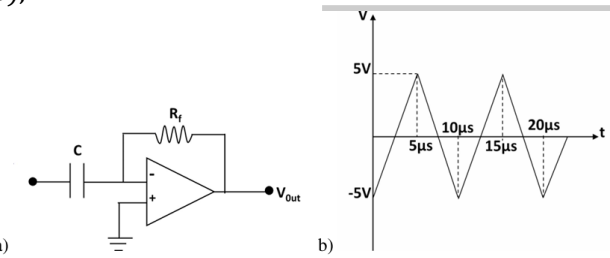
[JEST 2021]



The output waveform would be

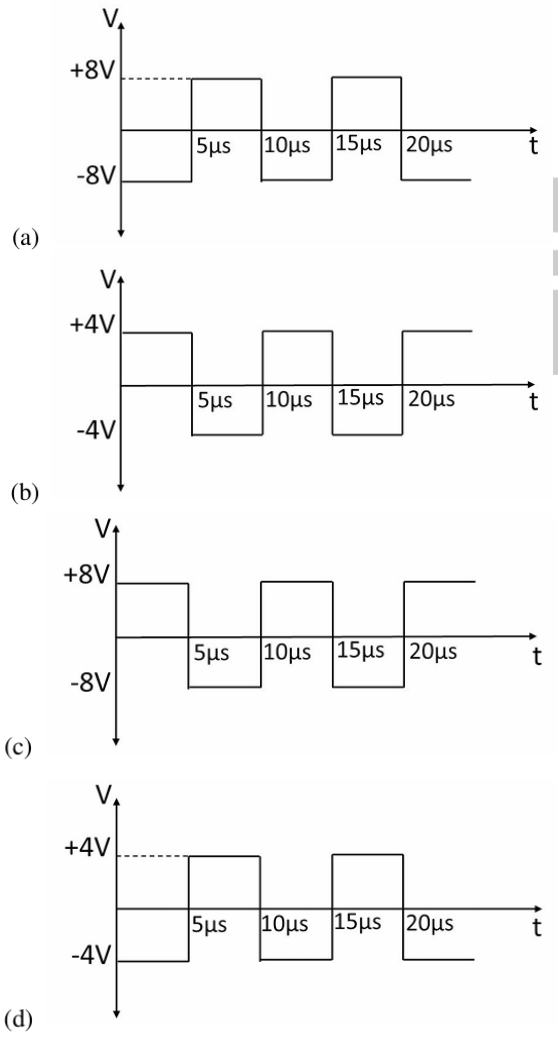


3. Consider the Op-Amp differentiator presented in Figure (a). Take $C = 0.002\mu$F and $R_f = 2$ kΩ. For a triangular wave input shown in the figure (b),



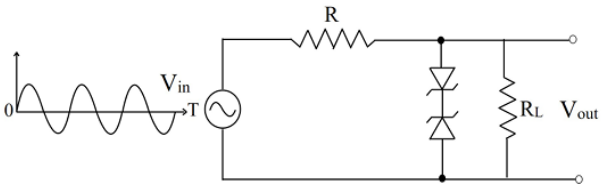
determine the output voltage waveform.

[JEST 2023]



4. What is the output waveform of the circuit for the given input signal? Assume that the zener diodes are identical, amplitude of the input voltage V_{in} is twice the zener breakdown voltage, and $R_L = 10R$.

[JEST 2024]

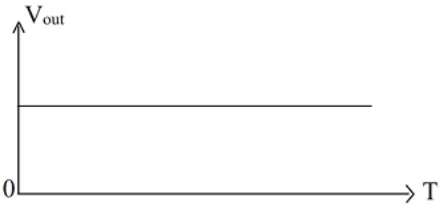


A.

B.

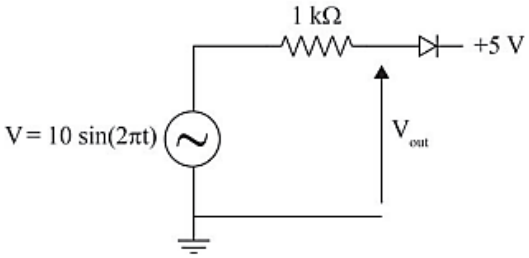
C.

D.

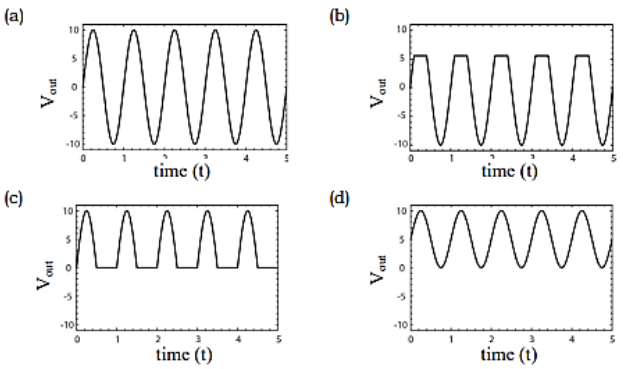


❖ TIFR PYQ

1. Consider the following circuit.



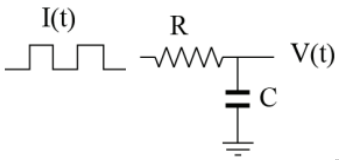
Which of the graphs given below is a correct representation of V_{out} ? **[TIFR 2014]**



2. Consider a sawtooth waveform which rises linearly from 0 Volt to 1 Volt in 10 ns and then decays linearly to 0 V over a period of 100 ns. Find the r.m.s. voltage in units of milliVolt?

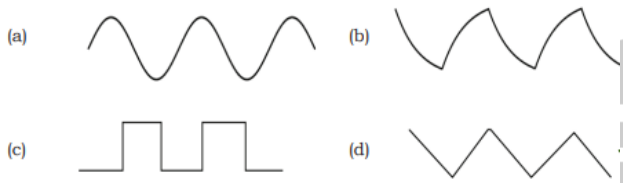
[TIFR 2016]

3. A current source produces a square wave $I(t)$ of 1.0 V peak-to-peak voltage and is used to drive the RC circuit shown below.

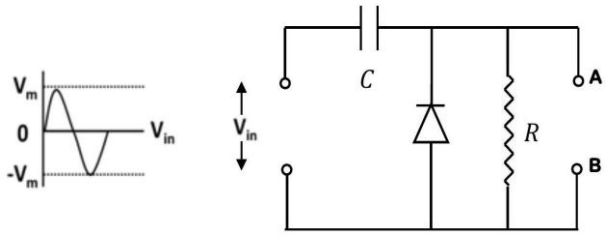


Which of the following represents the correct voltage across the capacitor C ?

[TIFR 2017]

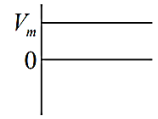


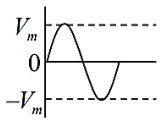
4. The signal shown on the left side of the figure below is fed into the circuit shown on the right side.

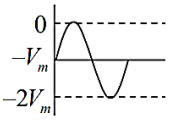


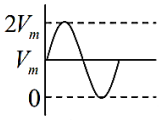
If the signal has time period τ_S and the circuit has a natural frequency τ_{RC}, then, in the case when $\tau_S \ll \tau_{RC}$, the steady-state output will resemble

[TIFR 2019]

(a) 

(b) 

(c) 

(d) 

❖ Answer Key				
CSIR-NET				
1. a	2. b	3. b	4. c	5. a
6. c	7. b			
GATE				
1. a	2. a	3. c	4. c	5. 3.16
6. a	7. a			
JEST				
1. b	2. a	3. a	4. a	
TIFR PYQ				
1. b	2. 577	3. d	4. d	

Frequency Modulation

❖ CSIR-NET PYQ

1. A live music broadcast consists of a radio-wave of frequency 7MHz, amplitude-modulated by a microphone output consisting of signals with a maximum frequency of 10KHz. The spectrum of modulated output will be zero outside the frequency band **[CSIR-DEC 2012]**

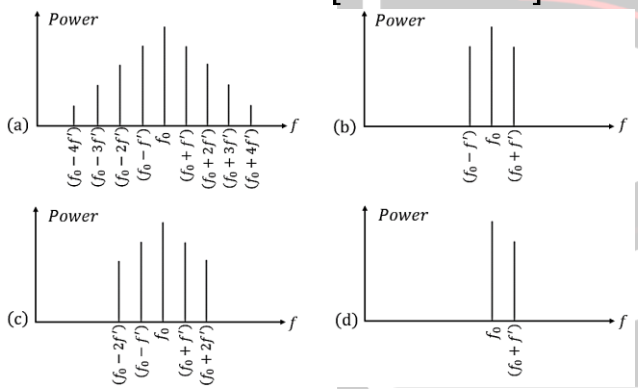
(a) 7.00MHz to 7.01MHz

(b) 6.99MHz to 7.01MHz

(c) 6.99MHz to 7.00MHz

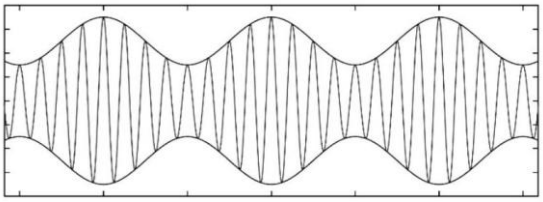
(d) 6.995MHz to 7.005MHz

2. The amplitude of a carrier signal of frequency f_0 is simusoidally modulated at a frequency $f' * f_0$. Which of the following graphs best describes its power spectrum? **[CSIR-DEC 2018]**



❖ TIFR PYQ

1. The figure below shows a carrier frequency 4kHz being amplitude-modulated by a sine wave signal.



In order to transmit the signal (without distortion) the minimum bandwidth needed would be **[TIFR 2020]**

(a) 8kHz (b) 2kHz

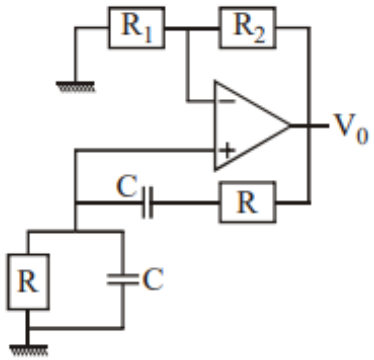
(c) 4kHz (d) 6kHz

❖ Answer Key

CSIR-NET				
1. b	2. b			
TIFR PYQ				
1. b				

❖ GATE PYQ

1. What should be the values of the components R and R_2 such that the frequency of the Wien Bride oscillator is 300 Hz ? [Given: $C = 0.01\mu F$ and $R_1 = 12k\Omega$] **[GATE 2004]**



(a) $R = 48k\Omega$ and $R_2 = 12k\Omega$

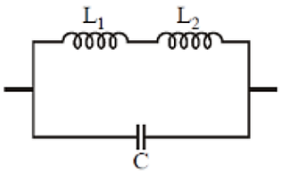
(b) $R = 26k\Omega$ and $R_2 = 24k\Omega$

(c) $R = 530\Omega$ and $R_2 = 1M\Omega$

(d) $R = 53k\Omega$ and $R_2 = 24K\omega$

2. The tank circuit of a Hartley oscillator is shown in the figure. If M is the mutual inductance between the inductors, the oscillation frequency is

[GATE 2006]



(a) $\frac{1}{2\pi\sqrt{(L_1 + L_2 + 2M)C}}$

(b) $\frac{1}{2\pi\sqrt{(L_1 + L_2 - 2M)C}}$

(c) $\frac{1}{2\pi\sqrt{(L_1 + L_2 + M)C}}$

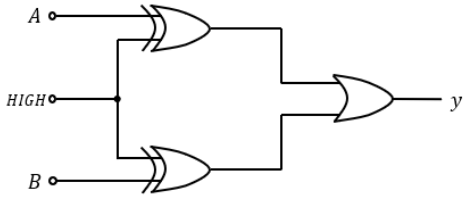
(d) $\frac{1}{2\pi\sqrt{(L_1 + L_2 - M)C}}$

❖ Answer Key				
GATE				
1. d	2. a			

❖ CSIR-NET PYQ

1. The logic circuit shown in the figure below. implements the Boolean expression

[CSIR-DEC 2012]



(a) $y = \overline{A \cdot B}$ (b) $y = \overline{A} \cdot \overline{B}$

(c) $y = A.B$ (d) $y = A + B$

2. A 4-variable switching function is given by $f = \Sigma(5,7,8,10,13,15) + d(0,1,2)$, where d is the donot-care-condition. The minimized form of f in sum of products (SOP) form is

[CSIR-DEC 2013]

(a) $\bar{A}\bar{C} + \bar{B}\bar{D}$ (b) $A\bar{B} + C\bar{D}$

(c) $AD + BC$ (d) $\overline{BD} + BD$

3. The truth table below gives the value Y(A, B, C), where A, B and C are binary variables.

A	B	C	Y
0	0	0	1
0	0	1	0
0	1	0	0
0	1	1	1
1	0	0	1
1	0	1	0
1	1	0	0
1	1	1	1

The output Y can be represented by

[CSIR-DEC 2018]

(a) $Y = \overline{A}\overline{B}C + \overline{A}B\overline{C} + A\overline{B}C + AB\overline{C}$

(b) $Y = \overline{A}\overline{B}\overline{C} + \overline{A}BC + A\overline{B}\overline{C} + ABC$

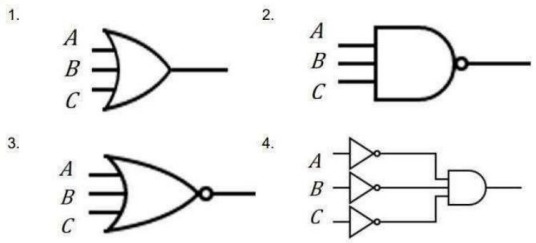
(c) $Y = \overline{A}\overline{B}C + \overline{A}BC + A\overline{B}C + ABC$

(d) $Y = \overline{A}\overline{B}\overline{C} + \overline{A}B\overline{C} + A\overline{B}\overline{C} + AB\overline{C}$

4. The logic circuit that will have the output

$$Y = (A + B)\overline{(\bar{A}(\bar{B} + \bar{C}))} + \bar{A}(B + C)$$

Is **[CSIR-DEC 2024]**



❖ GATE PYQ

1. Which of the given relations between the Boolean variables P and Q is NOT correct? (In the notation used here, P′ denotes NOT P and Q′ denotes NOT Q)

[GATE 2003]

(a) $PQ' + PQ = P$ (b) $(PQ)' = P' + Q'$

(c) $PQ' = (P' + Q)'$ (d) $PQ' + Q = P$

2. Which one of the set of values given below does NOT satisfy the Boolean relation $R = PQ'$ (where Q' denotes NOT Q)? **[GATE 2003]**

(a) $P = 1, Q = 1, R = 0$

(b) $P = 1, Q = 1, R = 1$

(c) $P = 0, Q = 0, R = 0$

(d) $P = 0, Q = 1, R = 1$

3. The Boolean expression $Y = \overline{A}\overline{B}\overline{C}D + \overline{A}\overline{B}CD + \overline{A}\overline{C}D + \overline{A}BCD$ reduces to **[GATE 2004]**

(a) $\overline{AB}$ (b) D

(c) $\overline{A}$ (d) $\overline{A}D$

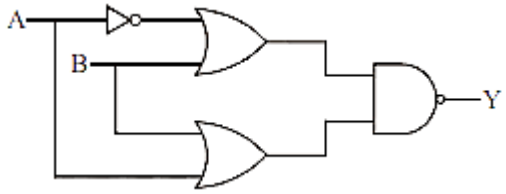
4. The Boolean expression: $B(A + B) + A \cdot (\bar{B} + A)$ can be realized using minimum number of

[GATE 2005]

(a) 1 AND gate (b) 2 AND gates

(c) 1 OR gate (d) 2 OR gates

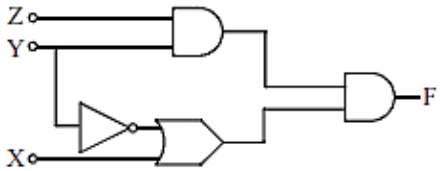
5. In the given digital logic circuit, A and B form the input. The output Y is **[GATE 2006]**



(a) $Y = \bar{A}$ (b) $Y = A\bar{B}$

(c) $Y = A \oplus B$ (d) $Y = \bar{B}$

6. Identify the function F generated by the logic network shown **[GATE 2007]**



(a) $F = (X + Y)Z$ (b) $F = Z + Y + \bar{Y}X$

(c) $F = ZY(Y + X)$ (d) $F = XYZ$

7. The minimized logic expression for the above map is **[GATE 2009]**

(a) $Y = \overline{PR} + \bar{Q}$ (b) $Y = \bar{Q} \cdot PR$

(c) $Y = \bar{Q} + PR$ (d) $Y = Q \cdot \overline{PR}$

8. The following Boolean expression

$$Y = A \cdot \bar{B} \cdot \bar{C} \cdot \bar{D} + \bar{A} \cdot B \cdot \bar{C} \cdot D + \bar{A} \cdot \bar{B} \cdot \bar{C} \cdot D + \bar{A} \cdot \bar{B} \cdot C \cdot D + \bar{A} \cdot B \cdot C \cdot D + A \cdot \bar{B} \cdot \bar{C} \cdot D$$

can be simplified to **[GATE 2011]**

(a) $\bar{A} \cdot \bar{B} \cdot C + A \cdot \bar{D}$ (b) $\bar{A} \cdot B \cdot \bar{C} + A \cdot \bar{D}$

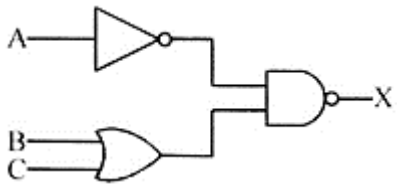
(c) $A \cdot \bar{B} \cdot \bar{C} + \bar{A} \cdot D$ (d) $A \cdot \bar{B} \cdot C + \bar{A} \cdot D$

9. Which one of the following does not represent an exclusive or operation for inputs A and B ? **[GATE 2015]**

(a) $(A + B)\overline{AB}$ (b) $A\bar{B} + B\bar{A}$

(c) $(A + B)(\bar{A} + \bar{B})$ (d) $(A + B)AB$

10. For the digital circuit given below, the output X is **[GATE 2016]**



(a) $\overline{\bar{A} + B \cdot C}$ (b) $\overline{\bar{A} \cdot (B + C)}$

(c) $\bar{A} \cdot (B + C)$ (d) $A + \overline{(B \cdot C)}$

11. The logic expression $\bar{A}BC + \bar{A}\bar{B}C + AB\bar{C} + A\bar{B}\bar{C}$ can be simplified to **[GATE 2018]**

(a) A XOR C (b) A AND C

(c) 0 (d) 1

12. Consider the following Boolean expression:

$$(\bar{A} + \bar{B})[\overline{A(B + C)}] + A(\bar{B} + \bar{C})$$

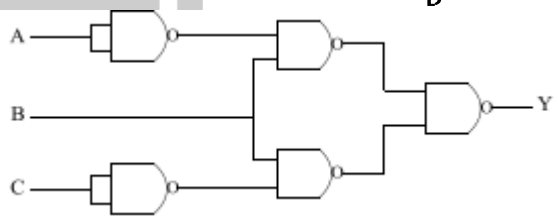
It can be represented by a single three-input logic gate. Identify the gate **[GATE 2019]**

(a) AND (b) OR

(c) XOR (d) NAND

❖ JEST PYQ

1. What is Y for the circuit shown below? **[JEST 2017]**



(a) $Y = \overline{(A + \bar{B})(\bar{B} + C)}$

(b) $Y = \overline{(A + \bar{B})(B + C)}$

(c) $Y = \overline{(\bar{A} + B)(\bar{B} + C)}$

(d) $Y = \overline{(A + B)(\bar{B} + C)}$

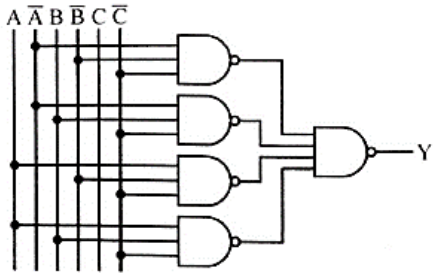
2. Let $ABCDEF$ be a regular hexagon. The vector $\overrightarrow{AB} + \overrightarrow{AC} + \overrightarrow{AD} + \overrightarrow{AE} + \overrightarrow{AF}$ will be **[JEST 2021]**

(a) 0 (b) $\overrightarrow{AD}$

(c) $2\overrightarrow{AD}$ (d) $3\overrightarrow{AD}$

❖ **TIFR PYQ**

1 The output (Y) of the following circuit will be **[TIFR 2017]**



(a) $\bar{A} + B + \bar{C}$ (b) $\bar{A}$

(c) $\bar{B}$ (d) $\bar{C}$

2 In Boolean terms, $(A + B)(A + C)$ is equal to **[TIFR 2018]**

(a) ABC

(b) $(A + B + C)(A + B)$

(c) $A(B + C)$

(d) $A + BC$

3 A three variable (A, B, C) truth table has a high output for the input conditions 000, 010, 100, and 110 and low otherwise. This effectively means the circuit following this truth table is the equivalent of **[TIFR 2021]**

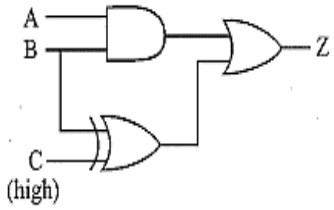
(a) $\bar{C}$ (b) $A + \bar{A}$

(c) A + B (d) $\bar{C}(A + B)$

❖ Answer Key				
CSIR-NET				
1. a	2. d	3. b	4. a	
GATE				
1. d	2. b,d	3. d	4. c	5. d
6. d	7. a	8.	9. d	10. b
11. a	12. d			
JEST				
1. a	2. d			
TIFR				
1. d	2. d	3. a		

❖ **CSIR-NET PYQ**

1. Consider the digital circuit shown below in which the input C is always high (I).



The truth table for the circuit can be written as

A	B	Z
0	0	
0	1	
1	0	
1	1	

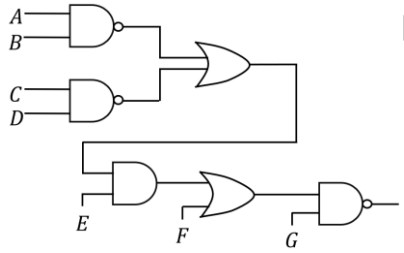
The entries in the Z column (vertically) are **[CSIR-JUNE 2011]**

(a) 1010 (b) 0100

(c) 1111 (d) 1011

2. The output 0, of the given circuit in cases I and II, where Case I : A, B = 1; C, D = 0; E, F = 1 and G = 0

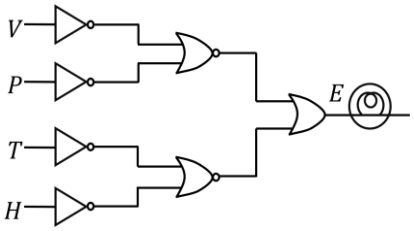
Case II : A, B = 0; C, D = 0; E, F = 0 and G = 1 are respectively **[CSIR-JUNE 2012]**



(a) 1,0 (b) 0,1

(c) 0,0 (d) 1,1

3. Four digital outputs V, P, T and H monitor the speed v, tyre pressure p, temperature t and relative humidity h of a car. These outputs switch from 0 to 1 when the values of the parameters exceed 85 km/hr, 2bar, 40°C and 50%, respectively. A logic circuit that is used to switch ON a lamp at the output E is shown below.



Which of the following conditions will switch the lamp ON? **[CSIR-JUNE 2013]**

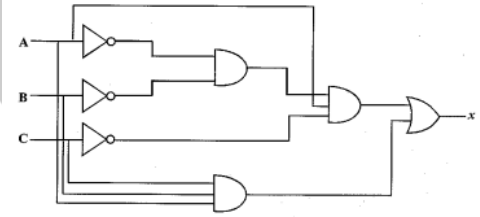
(a) v < 85 km/hr, p < 2 bar, t > 40°C, h > 50%

(b) v < 85 km/hr, p < 2bar, t > 40°C, h < 50%

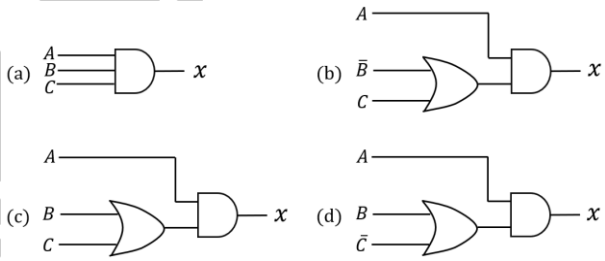
(c) v > 85 km/hr, p < 2bar, t > 40°C, h < 50%

(d) v > 85 km/hr, p < 2bar, t < 40°C, h > 50%

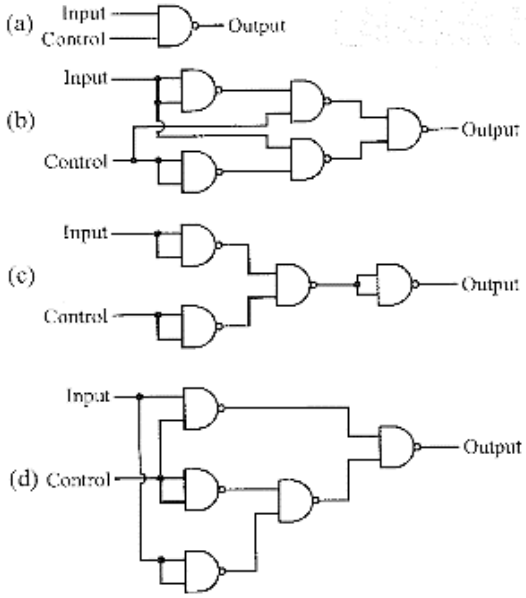
4. For the logic circuit shown in the figure below



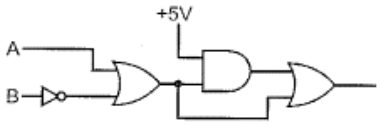
a simplified equivalent circuit is **[CSIR-JUNE 2014]**



5. Which of the following circuits behaves as a controlled inverter? **[CSIR-JUNE 2015]**



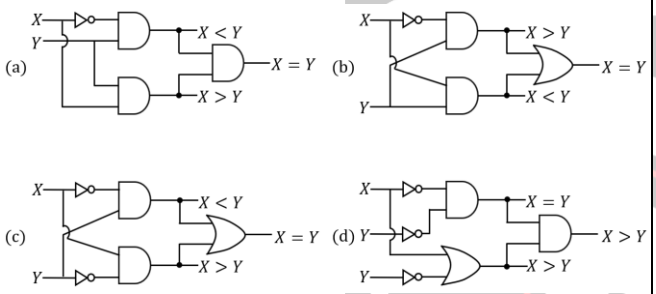
6. In the schematic figure given below, assume that the propagation delay of each logic gate is t_{gume}.
The propagation delay of the circuit will be maximum when the logic inputs A and B make the transition **[CSIR-JUNE 2016]**



(a) $(0,1) \rightarrow (1,1)$ (b) $(1,1) \rightarrow (0,1)$

(c) $(0,0) \rightarrow (1,1)$ (d) $(0,0) \rightarrow (0,1)$

7. In the figures below, X and Y are one bit inputs. The circuit which corresponds to a one bit comparator is **[CSIR-JUNE 2017]**



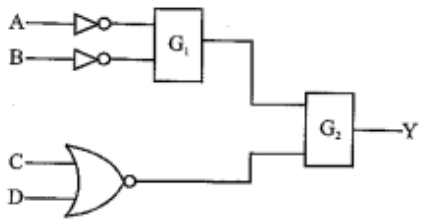
8. Which of the following gates can be used as a parity checker? **[CSIR-JUNE 2018]**
(a) an OR gate

(b) a NOR gate

(c) an exclusive OR (XOR) gate

(d) an AND gate

9. Let Y denote the output in the following logical circuit.



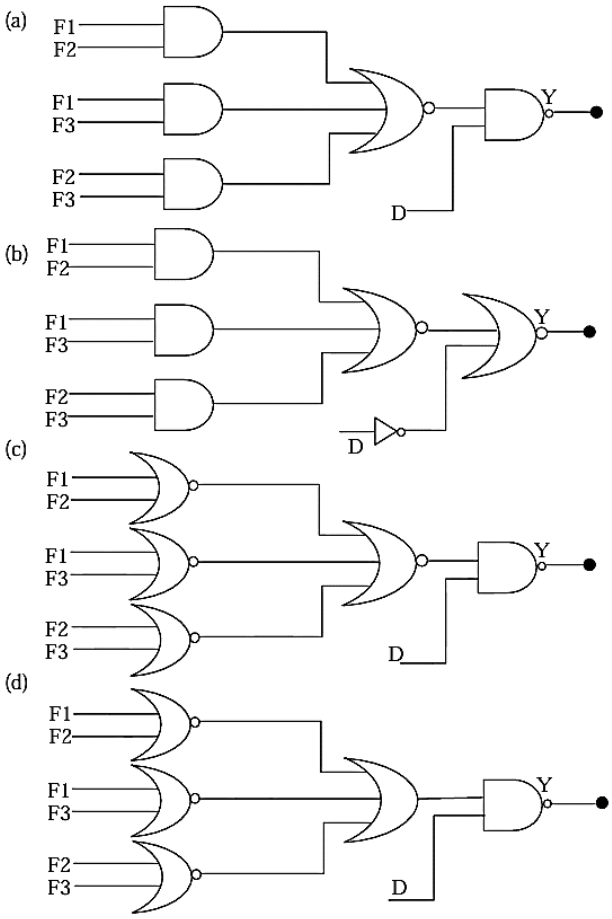
If $Y = AB + \bar{C}\bar{D}$, the gates G_1 and G_2 must, respectively, be **[CSIR-JUNE 2019]**
(a) OR and NAND (b) NOR and OR

(c) AND and NAND (d) NAND and OR

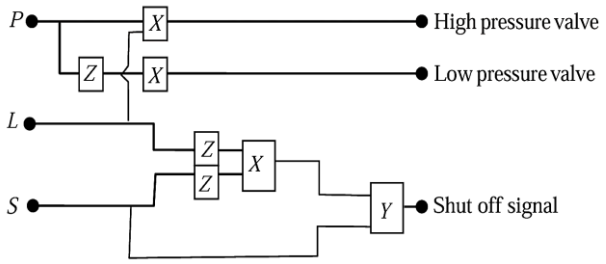
10. The Boolean equation $Y = \bar{A}BC + \bar{A}B\bar{C} + A\bar{B}\bar{C} + A\bar{B}C$ is to be implemented using only twoinput NAND gates. The minimum number of gates required is **[CSIR-JUNE 2020]**
(a) 3 (b) 4

(c) 5 (d) 6

11. The door of an X - ray machine room is fitted with a sensor D (0 is open and 1 is closed). It is also equipped with three fire sensors F_1, F_2 and F_3 (each is 0 when disable and 1 when enabled).
The X-ray machine can operate only if the door is closed and at least 2 fire sensors are enabled. The logic circuit to ensure that the machine can be operated is **[CSIR-JUNE 2021]**



12. A liquid oxygen cylinder system is fitted with a level-sensor (L) and a pressure-sensor (P), as shown in the figure below. The outputs of L and P are set to logic high (S = 1) when the measured values exceed the respective preset threshold values. The system can be shut off either by an operator by setting the input S to high, or when the level of oxygen in the tank falls below the threshold value.



The logic gates X, Y and Z, respectively, are **[CSIR-JUNE 2022]**

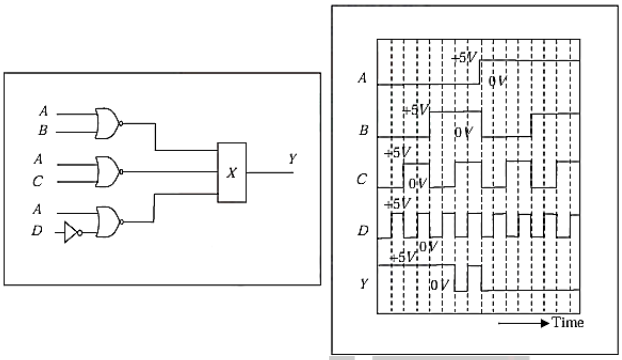
(a)OR, AND and NOT OR

(b)AND, OR and NOT

(c)NAND, OR and NOT

(d)NOR, AND and NOT

13. For the given logic circuit, the input waveforms A, B, C and D are shown as a function of time



To obtain the output Y as shown in the figure, the logic gate X should be **[CSIR-JUNE 2023]**

(a) 1 an AND Gate (b) an OR gate

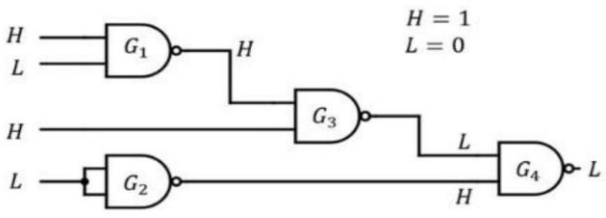
(c) a NAND gate (d) a NOR gate

14. For three inputs A, B and C, the minimum number of 2-input NAND gates required to generate the output $Y = \overline{A + B} + \bar{C}$ is **[CSIR-DEC 2023]**

(a)3 (b)4

(c)7 (d)6

15. The logic levels H and L at different locations in a digital circuit are found to be as shown in the figure.

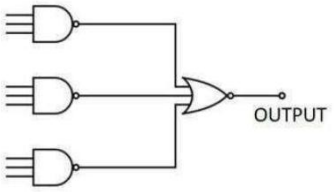


Based on these observations, which of the logic gates is not behaving as an ideal NAND gate? **[CSIR-JUNE 2024]**

(a)G_2 (b)G_3

(c)G_4 (d)G_1

16. The output of the following circuit is always found to be zero.



Such an observation can be due to **[CSIR DEC 2024]**

(a)Two of the inputs of any one of the NAND gates being accidentally shorted to each other

(b)One of the inputs to the NOR gate being accidentally grounded

(c)One of the inputs to one of the NAND gates being accidentally grounded

(d)Two of the inputs of the NOR gate being accidentally shorted to each other

❖ GATE PYQ

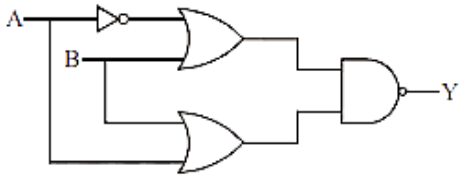
1. Draw the electrical circuits for each of the following ********** source (battery), a detector (lamp), and switch (es). **[GATE 2001]**

(a) AND (b) OR

(c) NOT (d) NAND

(e) NOR

2. In the given digital logic circuit, A and B form the input. The output Y is **[GATE 2006]**

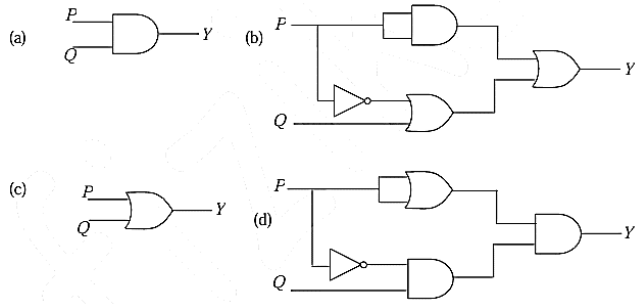


(a) $Y = \overline{A}$ (b) $Y = A\overline{B}$

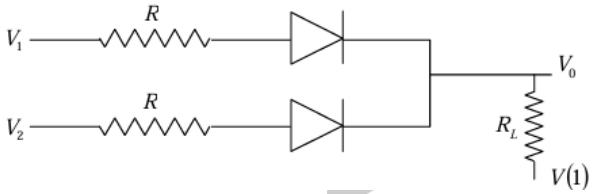
(c) $Y = A \oplus B$ (d) $Y = \overline{B}$

3. The simplest logic gate circuit corresponding to the Boolean expression, $Y = P + \bar{P}Q$ is

[GATE 2008]



4. The following circuit (where $R_L \gg R$) performs the operation of [GATE 2008]



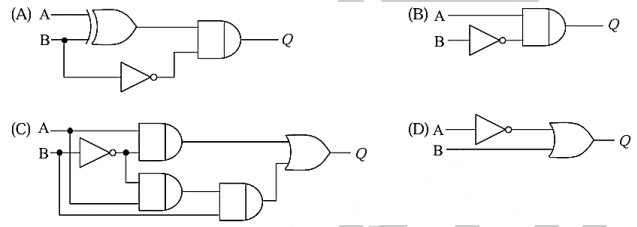
(a) OR gate for a negative logic system

(b) NAND gate for a negative logic system

(c) AND gate for a positive logic system

(d) AND gate for a negative logic system

5. For any set of inputs, A and B the following circuits give the same output, Q except one. Which one is it [GATE 2010]

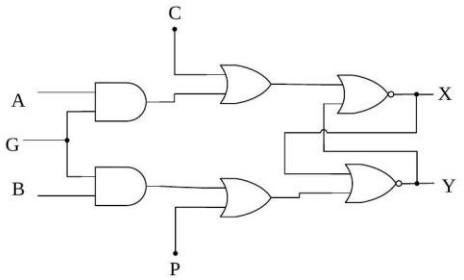


6. The minimum number of NAND gates required to construct an OR gate is [GATE 2017]

(a) 2 (b) 4

(c) 5 (d) 3

7. For the following circuit, the correct logic values for the entries X_2 and Y_2 in the truth table are [GATE 2019]



G	A	B	P	C	X	Y
1	0	1	0	0	0	1
0	0	0	1	0	X_2	Y_2
1	0	0	0	1	0	1

(a) 1 and 0 (b) 0 and 0

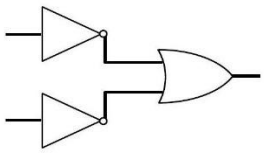
(c) 0 and 1 (d) 1 and 1

8. Which one of the following is a universal logic gate? [GATE 2020]

(a) AND (b) NOT

(c) OR (d) NAND

9.

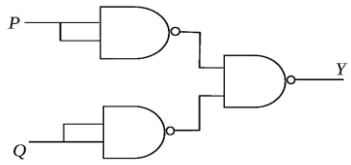


The above combination of logic gates represents the operation [GATE 2021]

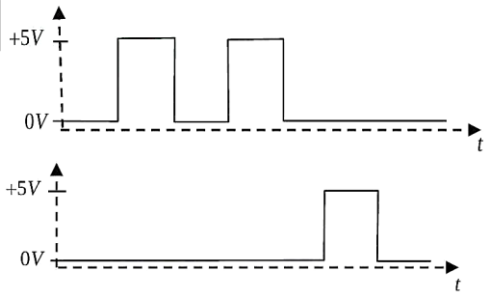
(a) OR (b) NAND

(c) AND (d) NOR

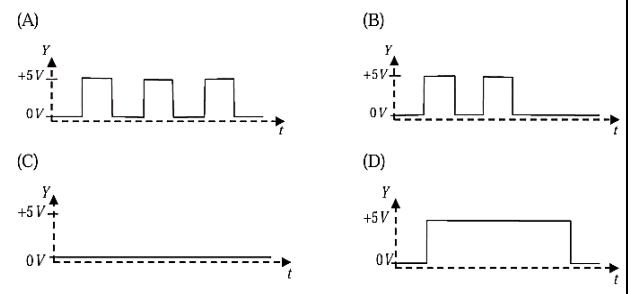
10. Consider the following circuit:



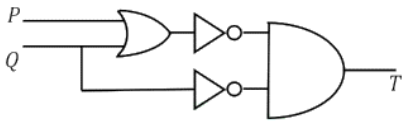
Suppose the input signal P is and the input signal Q is



Which one of the following output signals is correct? [GATE 2024]



11. A logic gate circuit is shown in the figure below. The correct combination for the input (P, Q) for which the output $T = 1$ is **[GATE 2025]**

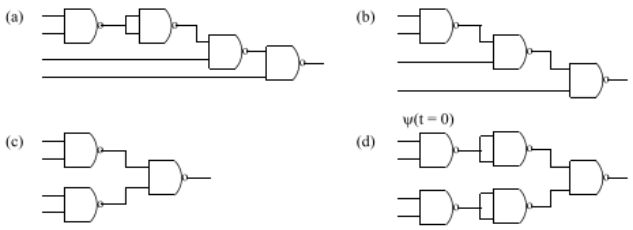


(a)(0,0) (b)(0,1)

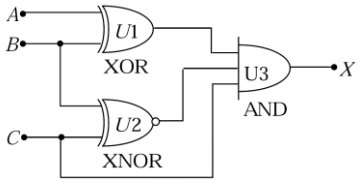
(c)(1,1) (d)(1,0)

❖ JEST PYQ

1. Which of the following circuits will act like a 4-input NAND gate? **[JEST 2014]**



2. For the logic circuit shown in figure 4, the required input condition (A, B, C) to make the output $(X) = 1$ is, **[JEST 2015]**



(a) 1,0,1 (b) 0,0,1

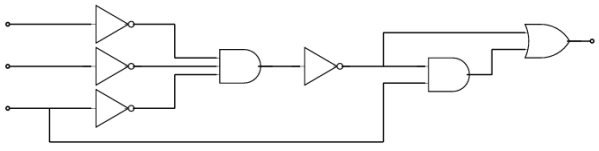
(c) 1,1,1 (d) 0,1,1

3. Consider all possible Boolean logic gates with 2 inputs and one output. How many such gates can be constructed? **[JEST 2023]**

(a) 16 (b) 4

(c) 2 (d) 8

4. What is the output of the following logic circuit? **[JEST 2024]**



(a) $X = A$ AND B AND C

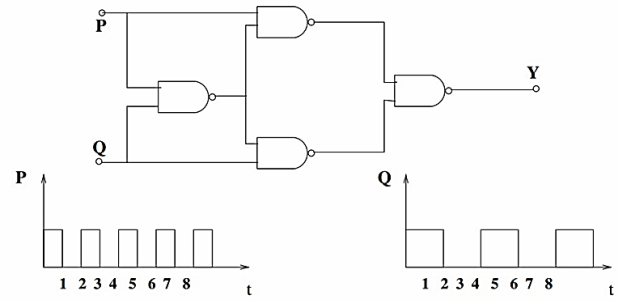
(b) $X = (A$ OR $C)$AND $(B$ OR $C)$

(c) $X = (A$ OR $C)$ AND $(B$ OR $C)$ AND C

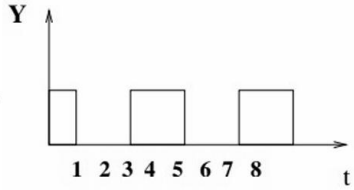
(d) $X = (\bar{A}$ OR $\bar{B}$ OR $\bar{C})$ AND C

5. The minimum number of basic logic gates required to realize the Boolean expression $B \cdot (A + B) + A \cdot (\bar{B} + A)$ is (in integer). **[JEST 2024]**

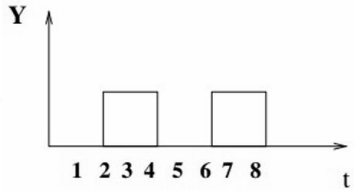
6. For the circuit and the inputs P and Q shown, which of the following is the correct output Y ? **[JEST 2025]**



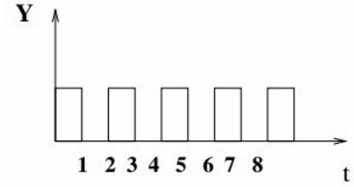
A.



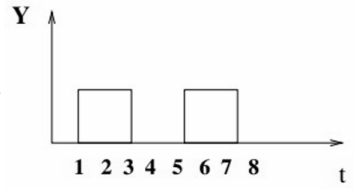
B.



C.



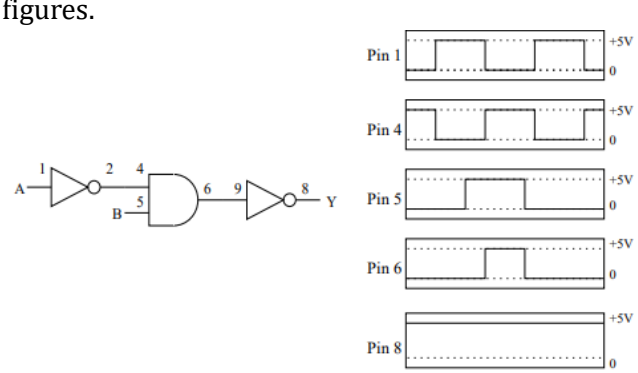
D.



❖ TIFR PYQ

1. The digital electronic circuit shown below (left side) has some problem and is not performing as intended. The voltage at each pin as a function of time is shown in the adjacent

figures.



The problem in the about circuit may be that **[TIFR 2011]**

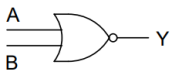
(a) the Pin 6 is shorted to ground

(b) the input inverter is shorted

(c) the Pin 8 is clamped to +5 V

(d) OR gate is used instead of AND gate

2. Consider the circuit shown below.



The minimum number of NAND gates required to design this circuit is **[TIFR 2012]**

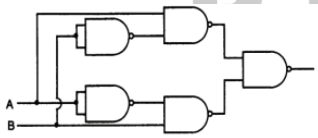
(a) 6 (b) 5

(c) 4 (d) 3

3. The circuit shown below uses only NAND gates. Find the final output. **[TIFR 2013]**

(a) A XOR B (c) A AND B

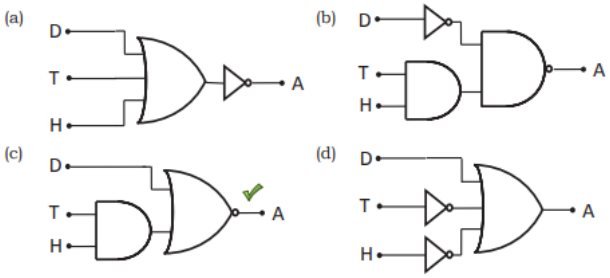
(b) A OR B (d) A NOR B



4. A control circuit needs to be designed to save on power consumption by an air-conditioning unit A in a windowless room with a single door. The room is fitted with the following devices:

1. a temperature sensor T, which is enabled ($T = 1$) whenever the temperature falls below a pre-set value;
2. a humidity sensor H, which is enabled ($H = 1$) whenever the humidity falls below a certain pre-set value;
3. a sensor D on the door, which is triggered ($D = 1$) whenever the door opens.

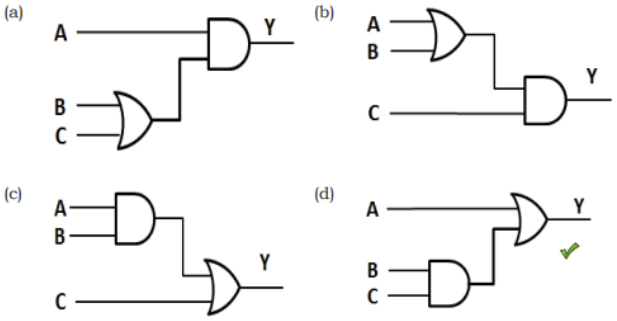
Which of the following logical circuits will turn the air-conditioning unit off ($A = 0$) whenever the door is opened or when both temperature and humidity are below their pre-set values? **[TIFR 2014]**



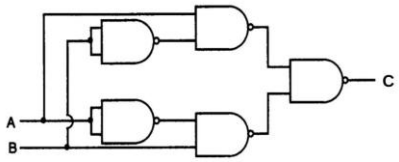
5. In a digital circuit for three input signals (A, B and C) the final output (Y) should be such that for inputs

A	B	C
0	0	0
0	0	1
0	1	0

the output (Y) should be low and for all other cases it should be high.
Which of the following digital circuits will give such output? **[TIFR 2016]**



6. The circuit shown below uses only NAND gates. **[TIFR 2019]**



The final output at **C** is

(a) A AND B (b) A OR B

(c) A XOR B (d) A NOR B

7. An OR gate, a NOR gate and an XOR gate are to be constructed using only NAND gates.

If the minimum number of NAND gates needed to construct OR, NOR and XOR gates is denoted $n(\text{OR}), n(\text{NOR})$ and $n(\text{XOR})$ respectively, then **[TIFR 2020]**

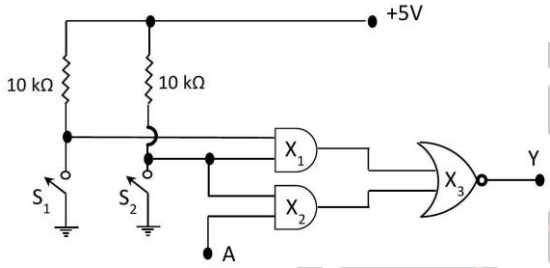
(a) $n(\text{NOR}) = n(\text{XOR}) > n(\text{OR})$ ↓

(b) $n(\text{NOR}) = n(\text{XOR}) = n(\text{OR})$

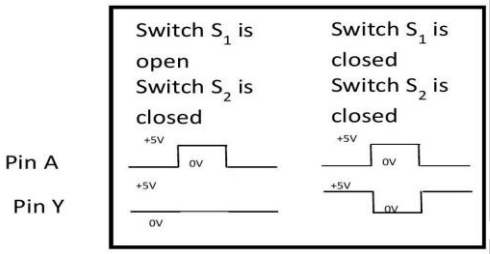
(c) $n(\text{NOR}) > n(\text{XOR}) > n(\text{OR})$

(d) $n(\text{NOR}) < n(\text{XOR}) = n(\text{OR})$

8. A sealed box containing a digital circuit has a circuit diagram pasted on its lid as shown below.



However, the output of the circuit is not as per this diagram. Some of the outputs actually obtained were as shown below **[TIFR 2021]**



Based on this we can conclude that the actual circuit inside has

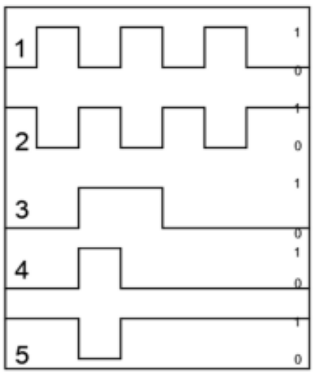
(a) OR gates instead of AND gates (X_1 and X_2)

(b) NAND gate instead of NOR gate (X_3)

(c) OR gate instead of NOR gate (X_3)

(d) AND gate instead of NOR gate (X_3)

9. A technician receives an electronic instrument on which the following circuit diagram is drawn. Based on the shown timing diagram (binary values at pins 1, 2, 3, 4, 5 as a function of time) measured by the technician, identify the fault in the instrument. **[TIFR 2024]**



Timing diagram

(a) Input inverter acts like an OR gate

(b) An AND gate is used where an OR gate should have been used

(c) Pin 4 shorted to ground

(d) Output inverter is faulty

10. The minimum number of two input NAND gates required to obtain the output $Y = \bar{A}B + \bar{C}$ from three inputs A, B and C is: **[TIFR 2024]**

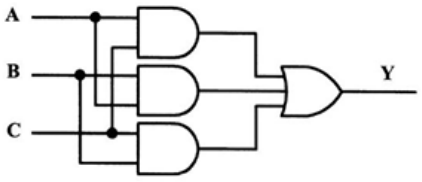
(a) 4 (b) 7

(c) 3 (d) 6

11. The output pulse train Y of the circuit shown on the right, with three synchronized input trains,

$A = 00001111$
$B = 00110011$
$C = 01010101$

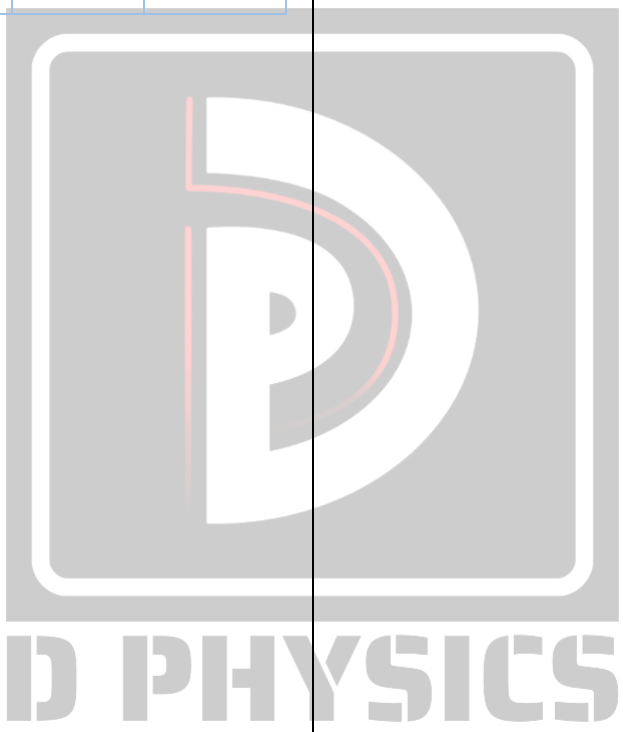
will be: **[TIFR 2025]**



(a) 00010111 (b) 00100111

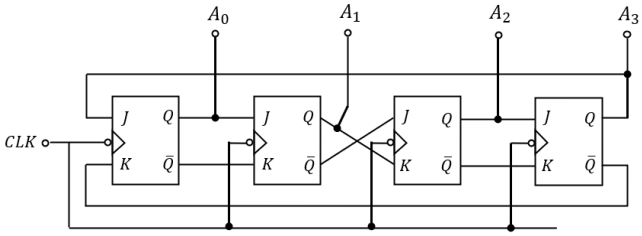
(c) 01010101 (d) 00010001

❖ Answer Key				
CSIR-NET				
1. d	2. d	3. a	4. a	5. b
6. d	7. c	8. c	9. b	10. b
11. b	12. b	13. b	14. b	15. c
16. c				
GATE				
1.	2. d	3. c	4. d	5. d
6. d	7. a	8. d	9. b	10. a
11. a				
JEST				
1. d	2. d	3. a	4. a	5. 1
6. d				
TIFR				
1.	2. c	3. a	4. c	5. d
6.	7. a	8. a	9. b	10. c
11. a				



❖ **CSIR-NET PYQ**

1. A counter consists of four flip-flops connected as shown in the figure.



If the counter is initialized as $A_0\ A_1\ A_2\ A_3 = 0110$, the state after the next clock pulse is **[CSIR-DEC 2011]**

(a) 1000 (b) 0001

(c) 0011 (d) 1100

2. If one of the inputs of a J-K flip flop is high and the other is low, then the outputs Q and $\bar{Q}$ **[CSIR-DEC 2013]**

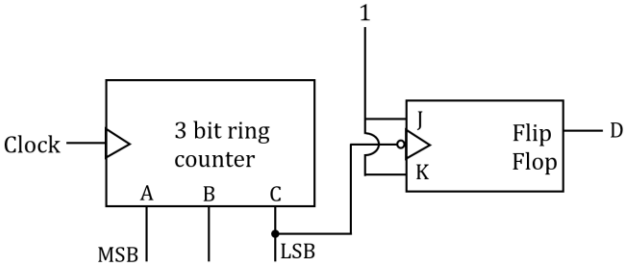
(a) oscillate between low and high in race-around condition

(b) toggle and the circuit acts like a T flip flop

(c) are opposite to the inputs

(d) follow the inputs and the circuit acts tike an R-S flip flop

3. For the logic circuit given below, the decimal count sequence and the modulus of the circuit corresponding to ABCD are **[CSIR-JUNE 2015]**



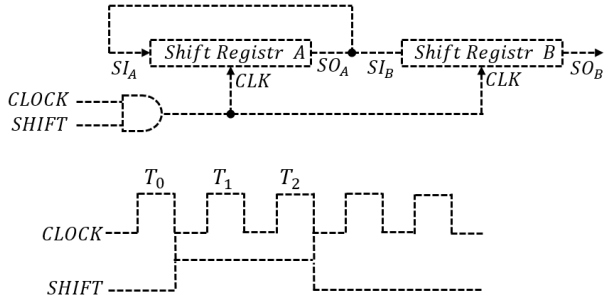
(a)$8 \rightarrow 4 \rightarrow 2 \rightarrow 1 \rightarrow 9 \rightarrow 5(\text{mod}6)$

(b) $8 \rightarrow 4 \rightarrow 2 \rightarrow 9 \rightarrow 5 \rightarrow 3(\text{mod}6)$

(c) $2 \rightarrow 5 \rightarrow 9 \rightarrow 1 \rightarrow 3(\text{mod}5)$

(d) $8 \rightarrow 5 \rightarrow 1 \rightarrow 3 \rightarrow 7(\text{mod}5)$

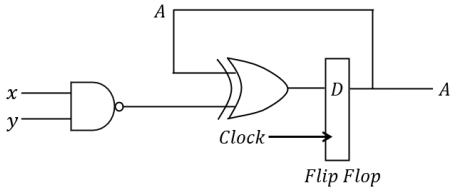
4. In the schematic figure given below, the initial values of 4 bit shift registers A and B are 1011 and 0010 respectively. The values of SO_A and SO_B after the pulse T_2 are respectively. **[CSIR-DEC 2015]**

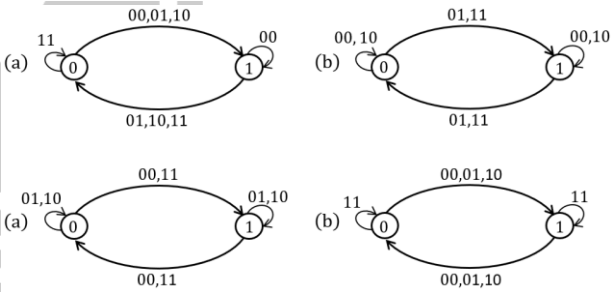


(a) 1110 and 1001 (b) 1101 and 100I

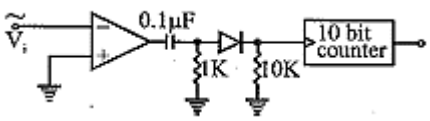
(c) 1101 and 1100 (d) 1110 and 1100

5. The state diagram corresponding to the following circuit is **[CSIR-DEC 2015]**





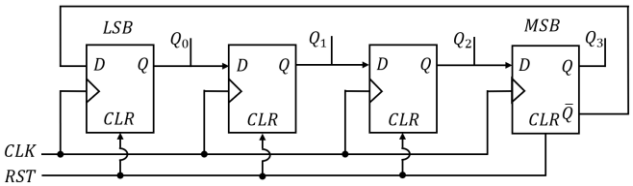
6. A sinusoidal signal of peak to peak amplitude 1 V and unknown time period is input to the following circuit for 5 seconds duration. If the counter measures a value $(3E8)_H$ in hexadecimal then the time period of the input signal is **[CSIR-DEC 2015]**



(a) 2.5 ms (b) 4 ms

(c) 10 ms (d) 5 ms

7. The circuit below comprises of D-flip flops. The output is taken from Q_3, Q_2, Q_1 and Q_0, as shown in the figure.



The binary number given by the string $Q_3Q_2Q_1Q_0$ changes for every clock pulse that is applied to the CLK input. If the output is initialized at 0000, then the corresponding sequence of decimal numbers that repeats itself, is

[CSIR-DEC 2017]

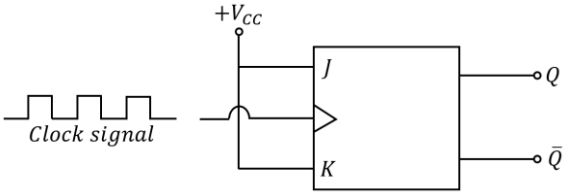
(a) 3,2,1,0

(b) 1,3,7,14,12,8

(c) 1,3,7,15,12,14,0

(d) 1,3,7,15,14,12,8,0

8. In the following JK flip-flop circuit, J and K inputs are tied together to $+V_{CC}$. If the input is a clock signal of frequency f, the frequency of the output Q is **[CSIR-JUNE 2018]**

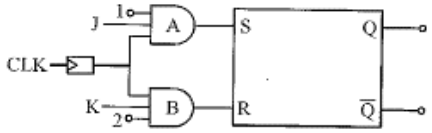


(a) f (b) $2f$

(c) $4f$ (d) $f/2$

9. Consider the following circuit, consisting of an RS flip-flop and two AND gates.
Which of the following connections will allow the entire circuit to act as a JKip-flop?

[CSIR-DEC 2018]



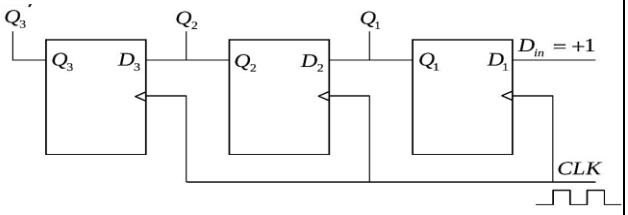
(a)connect Q to pin 1 and $\bar{Q}$ to pin 2

(b) connect Q to pin2 and $\bar{Q}$ to pin 1

(c) connect Q to K input and $\bar{Q}$ to J input

(d) connect Q to J input and $\bar{Q}$ to K input

10. In the 3-bit register shown below, Q_1 and Q_3 are the least and the most significant bits of the output, respectively.



If Q_1, Q_2 and Q_3 are set to zero initially, then the output after the arrival of the second falling clock (CLK) edge is **[CSIR-JUNE 2020]**

(a) 001 (b) 100

(c) 011 (d) 110

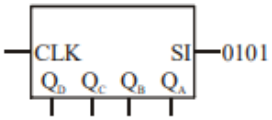
❖ GATE PYQ

1. A ripple counter designed with JK flip-flops provided with CLEAR(CL) input is shown in the figure. In order that this circuit functions as a MOD-12 counter, the NAND gate input (X_1 and X_2) should be **[GATE 2006]**

(a) A and C (b) A and D

(c) B and D (d) C and D

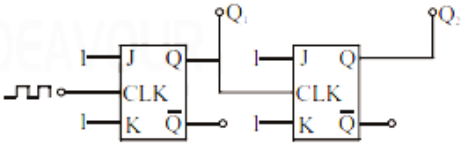
2. The registers Q_D, Q_C, Q_B and Q_A shown in the figure are initially in the state 1010 respectively. An input sequence SI = 0101 is applied. After two clock pulses, the state of the shift registers (in the same sequence $Q_DQ_CQ_BQ_A$) is **[GATE 2007]**



(a) 1001 (b) 0100

(c) 0110 (d) 1010

3. In the circuit shown, the ports Q_1 and Q_2 are in the state $Q_1 = 1, Q_2 = 0$. The circuit is now subjected to two complete clock pulses. The state of these ports now becomes **[GATE 2007]**

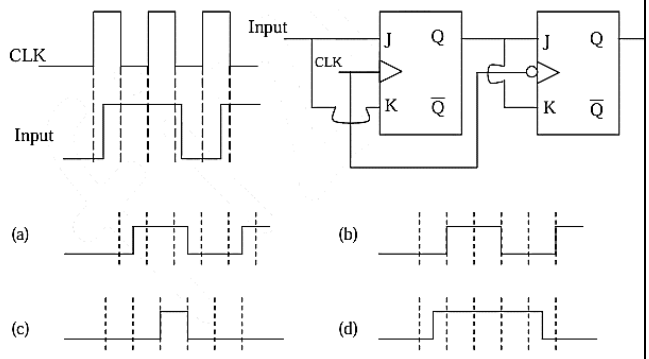


(a) $Q_2 = 1, Q_1 = 0$ (b) $Q_2 = 0, Q_1 = 1$

(c) $Q_2 = 1, Q_1 = 1$ (d) $Q_2 = 0, Q_1 = 0$

4. In the T type master slave JK flip flop is shown along with the clock and input wave forms. The Q_n output of flip flop was zero initially. Identify the correct output wave form

[GATE 2008]

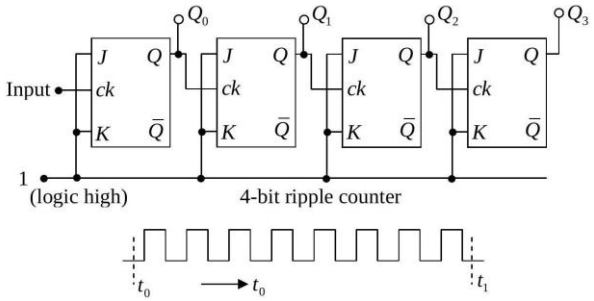


5. The minimum number of flip-flops required to construct a mod- 75 counter is.....

[GATE 2014]

6. Consider a 4-bit counter constructed out of four flip-flops. It is formed by connecting the J and K inputs to logic high and feeding the Q output to the clock input of the following flip-flop (see the figure). The input signal to the counter is a series of square pulses and the change of state is triggered by the falling edge. At time $t = t_0$ the outputs are in logic low state ($Q_0 = Q_1 = Q_2 = Q_3 = 0$). Then at $t = t_1$, the logic state of the outputs is

[GATE 2020]



Input signal

(a) $Q_0 = 1, Q_1 = 0, Q_2 = 0$ and $Q_3 = 0$

(b) $Q_0 = 0, Q_1 = 0, Q_2 = 0$ and $Q_3 = 1$

(c) $Q_0 = 1, Q_1 = 0, Q_2 = 1$ and $Q_3 = 0$

(d) $Q_0 = 0, Q_1 = 1, Q_2 = 1$ and $Q_3 = 1$

❖ **Answer Key**

CSIR-NET				
1. b	2. d	3. b	4. d	5. d
6. d	7. d	8. d	9. b	10. c
GATE				
1. d	2. a	3. c	4. a	5. 7
6. b				

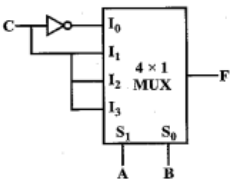
Combinational Circuits

❖ CSIR-NET PYQ

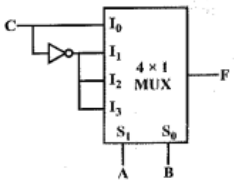
1. Which of the following circuits implements the Boolean function $F(A,B,C)$: $\Sigma(1,2,4,6)$?

[CSIR-DEC 2016]

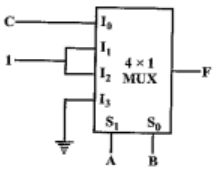
(a)



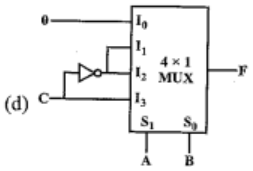
(b)



(c)



(d)



2. A 2 × 4 decoder with an enable input can function as a **[CSIR-JUNE 2017]**

(a) 4 × 1 multiplexer

(b) 1 × 4 demultiplexer

(c) 4 × 2 encoder

(d) 4 × 2 priority encoder

❖ GATE PYQ

1. A half-adder is a digital circuit with **[GATE 2004]**

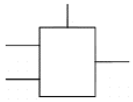
(a) three inputs and one output

(b) three inputs and two outputs

(c) two inputs and one output

(d) two inputs and two outputs

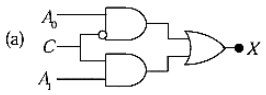
2. In a 2-to-1 multiplexer as shown below, the output $X = A_0$ if $C = 0$ and $X = A_1$ if $C = 1$.



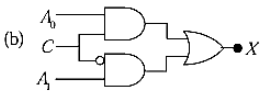
Which one of the following is the correct implementation of this multiplexer?

[GATE 2018]

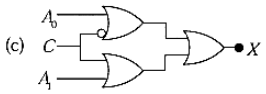
(a)



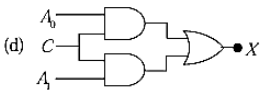
(b)



(c)



(d)



❖ TIFR PYQ

1. For exact calculation and minimum complexity, two four-digit binary numbers can be added with **[TIFR 2017]**

(a) 1 full adder and 3 half-adders

(b) 2 full adders and 2 half-adders

(c) 3 full adders and 1 half-adder ↓

(d) 4 full adders

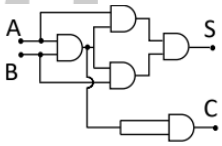
2. A half-adder circuit is defined as a two-input, two-output logic circuit where the output S gives the sum of inputs up to a single bit, and the output C gives carryover in a single bit.

The expected truth table of the half-adder is given as

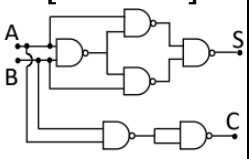
Input		Output	
A	B	S	C
0	0	0	0
0	1	1	0
1	0	1	0
1	1	0	1

Which of the following circuits does NOT behave like a half adder? **[TIFR 2023]**

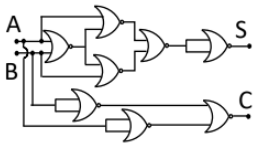
(a)



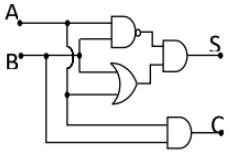
(c)



(b)



(d)



❖ Answer Key				
CSIR-NET				
1. b	2. b			
GATE				
1. d	2. a			
TIFR				
1. c	2. a			

Number System

❖ GATE PYQ

1. Which one of the following is the correct binary equivalent of the hexadecimal $F6C$? **[GATE 2020]**

(a) 011011111100 (b) 111101101100

(c) 110001101111 (d) 011011000111

❖ JEST PYQ

1. The 2' s compliment of 11111111 is **[JEST 2020]**

(a) 00000001 (b) 00000000

(c) 11111111 (d) 10000000

2. What is the 2′s complement representation of 11010110? **[JEST 2023]**

(a) 11010101 (b) 00101001

(c) 00101010 (d) 01101011

3. Convert the octal number 3720_8 to its decimal equivalent. **[JEST 2023]**

(a) 1000_{10} (b) 2000_{10}

(c) 2020_{10} (d) 1900_{10}

❖ TIFR PYQ

1. The pulse train at the output of an XNOR gate with the three inputs

$A = 00011011$
$B = 10100011$
$C = 00101110$

will be **[TIFR 2023]**

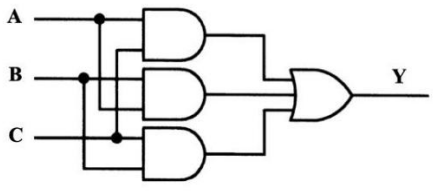
(a) 10101000 (b) 10010110

(c) 01010111 (d) 01101001

2. The output pulse train Y of the circuit shown on the right, with three synchronized input trains, **[TIFR 2025]**

$A = 00001111$
$B = 00110011$
$C = 01010101$

will be:



(a) 00010111 (b) 00100111

(c) 01010101 (d) 00010001

❖ Answer Key				
GATE				
1. b				
JEST				
1. a	2. c	3. b		
TIFR				
1. d	2. a			